REPORT #NSWC-95-6054-0006 5 May 1995

RADIATION TEST REPORT
Characterization Of Two Related Commercial Analog-to-Digital Converters: The AD872 and AD872A from Analog Devices, Inc.

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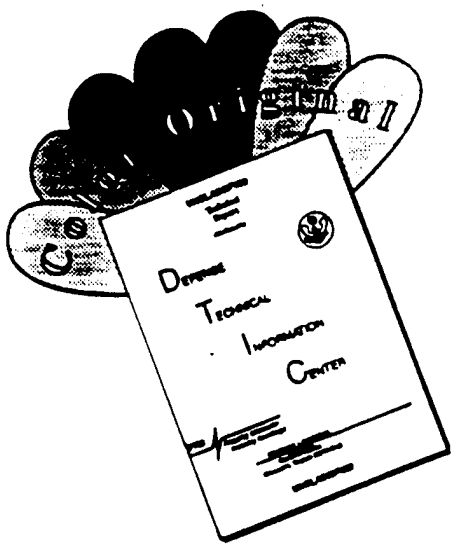

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AD872 & AD872A RADIATION TEST REPORT

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1.0 INTRODUCTION

1.1 Purpose

The purpose of these tests was to evaluate the dose rate and total dose susceptibility of the AD872 and AD872A Analog-to-Digital Converters (ADCs). The Advanced Technology Division of NSWC Crane tested the AD872 in both total dose and dose rate ionizing radiation environments. The AD872A was tested in the total dose environment. The results are contained in this report. This experiment was funded by the PMA-A1151 program of the U.S. Army Missile Defense, Space and Technology Center (USAMDSTC), in Huntsville Alabama.

1.2 Background

The AD872 and AD872A are closely related Analog-to-Digital Converters, manufactured by Analog Devices, Inc. (ADI) on their commercial ABCMOS technology. The AD872A is an improved-performance version of the AD872. The AD872 and AD872A are 12-bit, 10 Million-Samples-Per-Second (MSPS) monolithic converters and share an identical architecture and many internal design features with the radiation-hardened AD9872 ADC built on the hardened RBCMOS technology. Both commercial ADCs, and the hardened ADC share a 4-stage feed-forward series/parallel architecture, as described in section 1.3.2. Because of the shared design features of these devices, the commercial ADC should exhibit radiation characteristics better than most commercial devices, and thus be a prime candidate for the sub-elements of National Missile Defense (NMD), and Theater Missile Defense (TMD) which must operate in a radiation environment. The sub-elements which must withstand more rigorous radiation requirements should find the radiation-hardened AD9872 a strong candidate for these applications. Current plans call for comprehensive radiation testing of the AD9872 during FY95.

The PMA-A1151 program initiated a program with Analog Devices, Inc., Wilmington, MA, in 1988 to develop radiation-hardened ADCs. The first step was to develop a hardened process. ADI chose to harden a main-line commercial technology which integrated bipolar NPN transistors and 2 micron CMOS on a single monolithic technology. The commercial technology is called advanced bipolar CMOS (ABCMOS), and the radiation-hardened variant is called radiation bipolar CMOS

(RBCMOS). From the beginning, attempts were made to minimize the differences between ABCMOS and RBCMOS, in terms of its process flow. RBCMOS requires one additional mask, and about 5% more processing steps than ABCMOS.

One of the first parts developed was a 10-bit, 18 MSPS ADC, the AD973. Its commercial equivalent was the AD773. Also, another device developed on the program was a 12-bit 10 MSPS ADC, which utilized an ADI-internal name of RBC12. From this device the AD872 commercial ADC was developed. This part has had significant commercial success and is widely used in commercial imaging and medical applications. Combining both commercial and radiation-based (from the PMA-A1151 program) design improvements, an improved version, the AD872A was released in 1995. The AD9872 radiation-hardened version of the AD872A is currently undergoing manufacturing qualification at ADI and is expected to be released in August 1995.

1.3 Test Specimens

1.3.1 Test Samples

Test samples used in this experiment contain both AD872's screened to the "S" military temperature range, -55°C to +125°C, marked AD872SD (date code 9421); and AD872A's, screened to "J" commercial temperature range, 0°C to 70 °C, marked AD872AJD (date code 9451). Eleven AD872 samples, and three AD872A samples were available for testing. The test samples were packaged in 28-PIN ceramic DIPs.

1.3.2 AD872 and AD872A Design Features

The AD872 and AD872A designs utilize a 4-stage pipelined multiple flash architecture, as shown in Figure 1.

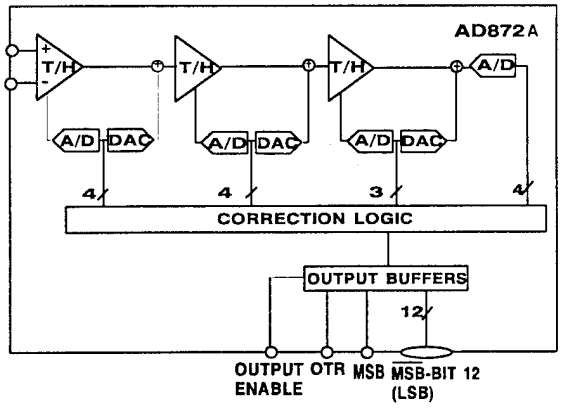

Figure 1. AD872A and AD872 Architecture

At the package level, there is no functional difference between the parts, only improved electrical performance for the AD872A. The analog input is a fully differential track and hold amplifier (THA). A 4-bit digital approximation of the input is made by the first flash converter, and an accurate 4-bit analog representation of the first flash output is generated by a 12-bit accurate digital-to-analog converter (DAC). The DACs analog output is subtracted from the THA output to create a remainder, or residue. The second THA captures this residue, which is converted by a second 4-bit flash ADC. Once the second THA captures the residue, the first THA captures a new input signal. All ADC outputs are captured in digital registers, with appropriate pipeline depth to synchronize the flash outputs. A second DAC output is subtracted from the THA output and passed to a third THA. The third stage flash is a 3-bit design. Its output is stored and the third DAC creates a third residue. This is passed to a final 4-bit ADC by the third THA. The 15 bit output by the 4 flashes are passed through correction logic and the optimal 12-bit representation of the analog signal is output.

Note that, while a new input is sampled every 100ns (for a 10 MHz clock), the output corresponding to a particular input signal is delayed by 4 clock cycles due to the pipeline architecture of the design. This pipeline delay is called latency, and the AD872 and AD872A both exhibit a latency of 4. The device is controlled by a single external clock input. Since the signal accuracy depends upon the stored analog signals in the THAs, a minimum clock rate of 10 kHz is required to avoid signal droop. The high-impedance differential input maintains a bandwidth significantly above Nyquist frequency. The part also has an Out of Range (OTR) output signal to indicate samples where the input exceeds the +/- 1 volt analog input range.

The AD872 and AD872A feature an internal 2.5 volt voltage reference output which may be connected to the ADCs reference input. This internal reference is based upon a bandgap design and is not radiation-hardened. Total dose tests were performed using both the internal and an external voltage reference. The dose rate tests used only an external reference.

1.3.3 AD872 and AD872A Specifications

	AD872	AD872A
Resolution	12-bit	12-bit
Speed	10 MSPS	10 MSPS
Power	1.15 Watt	1.03W
Analog Input	+/- 1 Volt	+/- 1 Volt
DNL	+/- 0.5 bits	+/- 0.5 bits
SNR	64 dB	69 dB
SINAD	61 dB	68 dB
THD	-68 dB	-74 dB
SFDR	72 dB	75 dB
IMD	-70 dB	-80 dB

See Appendix B for Manufacturer's Specification Sheet.

2.0 SUMMARY

2.1 Total Dose

Four AD872s showed initial degradation between 50KRads(Si) and 150KRad(Si) with a static bias, and one AD872A showed initial degradation at approximately at 250KRads(Si) with a static bias.

2.2 Dose Rate

The AD872 dose rate results show the onset of upset at 1E7 to 5E7 Rad(Si)/sec, and all bits upset at 5E9 Rad(Si)/sec. No latchup was observed at 8E11 Rad(Si)/sec at 25°C.

3.0 REFERENCES

USASSDC Testing Guidelines for Radiation Hardened VLSI(U), September 1992, Sensors Directorate, Active Sensors Division

MIL-STD-883 Test Methods and Procedures for Microcircuits

4.0 TOTAL DOSE TEST RESULTS

4.1 Test Facility

The AD872's and AD872A's were tested in the Crane Shepherd Model 484 Cobalt-60 Irradiator. The dose rate was 60.8 rad(Si)/sec for the first experiment and 92.5 rad(Si)/sec for the second experiment, as described in section 4.2. Using a lead-aluminum enclosure to shield low energy radiation, one sample was exposed at a time, in compliance with Test Method 1019.4.

4.2 Dosimetry

CaF TLD dosimeters were taped to the device socket which was contained in a lead aluminum box to eliminate low energy X-rays and comply with test method 1019.4. Using approximate data from earlier experiments, 3 positions were monitored by exposing a TLD to the 8000 curie source for one minute. A control TLD was exposed for one minute to radiation in the AEC-Canada Gamma-Cell source at Crane which, due to known experimental geometry of the Gamma-Cell, provides an accuracy check. The TLDs were read using Crane's ALNOR RE1. The first experiment used a dose rate of 60.8 rad(Si)/sec which correspond to a position of 90mm from the

source. The second experiment used a dose rate of 92.5 rad(Si)/sec which corresponds to a position of 60mm from the source.

4.3 Test Procedure

The test plan called for two test conditions: 1) static biased condition, in which the clock and analog inputs were grounded and the device powered with nominal values, and 2) dynamic condition where the device is clocked at 10MHz and the analog input is a 1 MHz sine wave with full scale input amplitude.

Functional tests were developed on both the MADCAT Test System and the Intelligent Instruments Test System. Parametric tests for power supply currents, output voltage and currents and the internal voltage reference were developed on the Eagle LSI-5 test system.

Three AD872's were exposed in the static bias condition using an external voltage reference. One AD872 and one AD872A using a static bias and external voltage reference, one AD872 and one AD872A using a dynamic bias and external voltage reference and one AD872 and one AD872A using dynamic bias with an internal voltage reference.

4.4 Defining ADC Failure

Functional failure in an ADC is somewhat subjective. For a particular application, a very small shift in dynamic parameters such as integral non-linearity (INL), differential non-linearity (DNL), signal-to-noise ratio (SNR), spurious-free-dynamic-range (SFDR) and total harmonic distortion (THD) may be critical. While a test can be tailored to a specific critical parameter, it is not practical to test and extract exact data on all critical parameters while minimizing radiation annealing. The following total dose results discuss the first observed significant degradation in ADC performance. For the AD872 and AD872A, functional degradation was always observed prior to any parametric shift. Significant degradation was defined as either missing codes, visible change in histogram data, or a reduction in SNR of more than 6 dB, or 1 effective number of bits (ENOB).

4.5 Test Results

4.5.1 Summary of Data

A total of six AD872s and 3 AD872As were tested at a moderate dose rate (60-90 rad(Si)/sec). Several bias conditions were used during radiation exposure. A static (unclocked with power on) condition was worst case for both device types. When operating in a dynamic bias, with clock applied and an AC input signal, significantly

better results were observed. These data use an external voltage reference. When the internal reference provided on the chip is used, the degradation of the reference becomes the dominant factor. The details of the two experimental exposures are provided in sections 4.5.2 and 4.5.3, but a summary of the results follow.

The worst case data where a static bias was used is summarized in Figure 2. Of the five devices tested, four were AD872s and one was an AD872A. The critical data is in the shaded with lines slanted from lower left to upper right (yellow), which shows the range from the last observed irradiation point with no significant degradation, to the first observation of device degradation. Looking at devices AD03, AD04 and AD05, first degradation would be expected between 70 and 100 KRad(Si) (due to a test problem, the data a 50 KRad(Si) was not recorded on AD03, but the 100 KRad(Si) data reinforces the data of AD04 and AD05). The data for AD02 is higher, with the device passing at 100 KRad(Si), and degradation observed at 150 KRad(Si). The test procedure for AD05 differed from AD02-AD04, to reduce annealing effects. AD02 had six interim data levels recorded, each requiring the device to be out of radiation for 15 minutes. While AD02 could be within the high side of the AD872s distribution, annealing during the test probably accounts for the higher level observed. While this sample is small, a conservative estimate of the AD872s hardness is 50 KRad(Si). The AD872A represents a notable redesign of the AD872, as discussed in section 1.3.2. While these changes were made primarily for improved electrical performance, their effect on radiation performance is significant. The single AD872A tested with a static bias degraded between 240 and 250 KRad(Si). While no statistical inference can be drawn from a single part, it appears that the AD872A will exceed a 100 KRad(Si) radiation tolerance in the worst case static bias.

Both device types were also tested with a dynamic bias, as shown in Figure 3. A second variable, the use of the internal voltage reference was also checked while maintaining the dynamic ADC bias. First, look at the two devices that utilized an external voltage reference. The AD872 (AD06) did not display degradation until 300 KRad(Si), compared to 80 KRad(Si) for AD05 with a static bias. The AD872A (AD13) performed remarkably, finally degrading at 800 KRad(Si). Both device types share many layout features with the radiation-hardened AD9872, which may account for some of the observed hardness, but both device types demonstrated outstanding tolerance for a commercial process. Even with a large variance in radiation performance, it is reasonable to assume a population of AD872s will exceed 100 KRad(Si). The AD872As appear even harder, but more tests are required to verify such a high level of radiation tolerance on a commercial device. The internal reference is a bandgap type, which typically do not perform well with radiation. When the ADCs were irradiated utilizing the internal reference, the response of the reference dominated the experiment. For the AD872 (AD07), the degradation level of 80 KRad(Si) is similar to the static biased AD05, but the failure mode was different. The AD872A (AD14) first degraded at 280 KRad(Si), also a level similar to the static

biased AD12. The combined effects of static bias and the internal reference potentially will lower the worst case static bias level for both device types.

4.5.2 First Experiment

The first experiment exposed three AD872's using a static bias and external voltage reference. Since the parts radiation response was not known small irradiation steps were planned to determine the first electrical failure and the expected failure level. The static bias has been demonstrated to be the worst case bias in related parts. At each interval the part was removed from the cell, and tested on all three testers. This resulted in the parts being out of the cell about 15 minutes at each step with the irradiation lasting only a few minutes. As will be discussed, there were indications in the data that the device was annealing during the test interval. Functional electrical tests were done with nominal power supplies (+/- 5 volts) and full scale AC input voltage (+/- 1 volt peak-peak). Exposure continued beyond first degradation, often with modified operating parameters to determine failure modes and observe further degradation.

As shown in Figure 2, the parts were harder than anticipated. Serial number AD02 was tested first. The part passed all electrical tests at 5, 10, 20, 30, 50, 80 and 100 KRad(Si). These results are shown by the gray (green) shaded bar in figure 2. A significant failure occurred at 150 KRad(Si), when over 100 missing codes were registered, gray bar slanted from lower left to upper right bar (yellow), indicates first failure occurred between 100 and 150 KRad(Si)). A missing code indicates the converter never registers that particular code while collecting data that previously included that particular code. At 200 KRad(Si) a few additional errors occurred, but when the power supplies were increased to greater than the nominal +/-5 volts, and the input sine wave's amplitude was decreased slightly, the part resumed operation. The purpose of these modified operating parameters was to isolate the failure mode of the AD872. Previous experience with radiation-hardened ADC similar to the AD872 demonstrated that functional failure was caused by loss of signal headroom, or allowable operating range of the internal signal, in the sample and hold amplifiers. When the power supplies were increased, and/or the input voltage range reduced, the part again had sufficient headroom, and appeared functional. These tests therefore show the cause of failure, and do not indicate a reduced operating region of interest to a system. The 200, 300 and 500 KRad(Si) exposures all demonstrate this modified functionality, as shown by the gray bar (red). At 1 MRad(Si), the part was non-functional, and did not recover with parameter modification.

The second part tested was AD03. The first interval tested was 100 KRad(Si). Over 200 missing codes were observed at this level, so no undegraded post-irradiation data, gray bar (green) was recorded for this device. As before the part would operate with

adjusted test conditions at 150, 200, 300 and 500 KRad(Si). The device was non-functional (as opposed to degraded but operating) at 700 and 1000 KRad(Si).

The third part tested was AD04. To balance the suspected annealing observed in AD02 and the early failure of AD03, this device was tested at 50 KRad(Si) intervals until degradation was observed. The device passed at 50 KRad(Si), but exhibited missing codes at 100 KRad(Si). From this data it cannot be positively inferred if the earlier failure level is a result of less annealing or of part-to-part variation. Continued test intervals at 150, 400 and 600 KRad(Si) showed the part worked with modified parameters. The part was non-functional at 800 and 1000 KRad(Si).

The primary conclusion to be drawn from the first experiment is that the AD872 is probably usable in a system with a 50 KRad(Si) specification. With the small sample size and the intervals selected, this is the only conclusion warranted. Device AD02, which passed at the 100 KRad(Si) level, had 6 step electrical tests during that interval. This means the device was out of radiation for about 1.5 hours and in the radiation field for less than 0.5 hours. It is reasonable to assume that annealing played a role in this test data. As noted, the radiation test intervals used for AD03 and AD04 were modified to lessen the effects of experiment-induced annealing. The second experiment modified the planned electrical test to reduce the test time.

During the first experiment, parametric data was collected on the power supply currents, digital output drive levels, and the internal (bandgap) voltage reference which is integral to the chip. Only the internal voltage reference displayed significant change. In the interval between 0 and 100 KRad(Si), no significant changes were found in power supply currents or the output voltage levels of the digital outputs. Above 100 KRad(Si), (a) very minor changes are noted in the output voltage levels (they remain well within specification), and (b) the total device power is reduced, probably due to reduced functional range of some sub-blocks within the device.

The first experiment utilized an external voltage reference to power the ADC. However, the output voltage of the internal voltage reference on the chip was monitored. The internal reference is a bandgap reference, which establishes a reference based upon the difference in base to emitter voltage drops of two transistors of different size, traditionally have performed poorly in radiation environments. As shown in Figure 4, the AD872 and AD872A references degrade significantly with total dose. This data shows the output reference voltage versus dose for the devices with no current load applied to the output. No load is the best condition for a reference. The reference is rated at 2 mA output and will be loaded in later tests. The part gracefully degrades some 70 mV over 1 MRad(Si) of radiation.

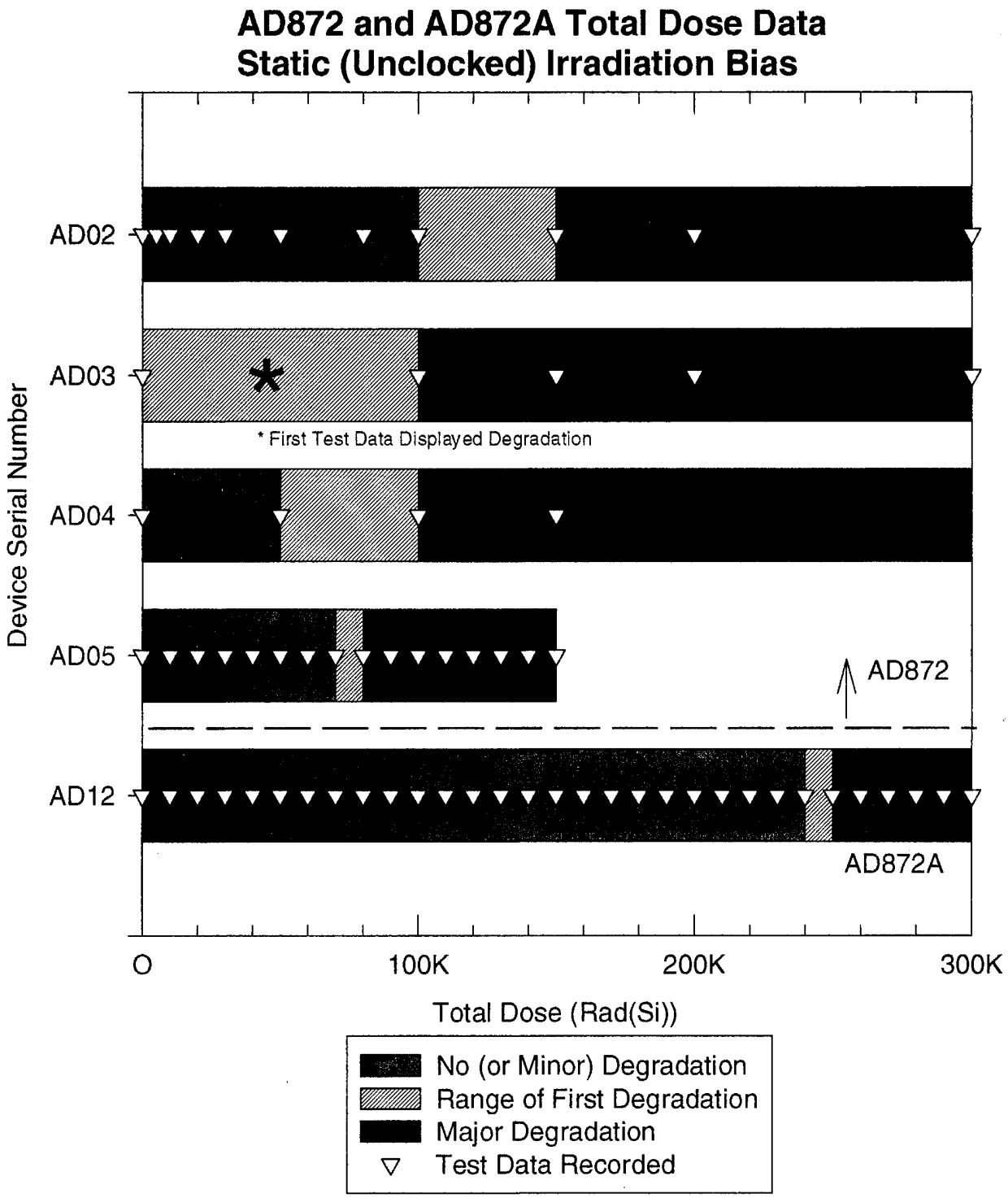

Figure 2. Static Bias Results

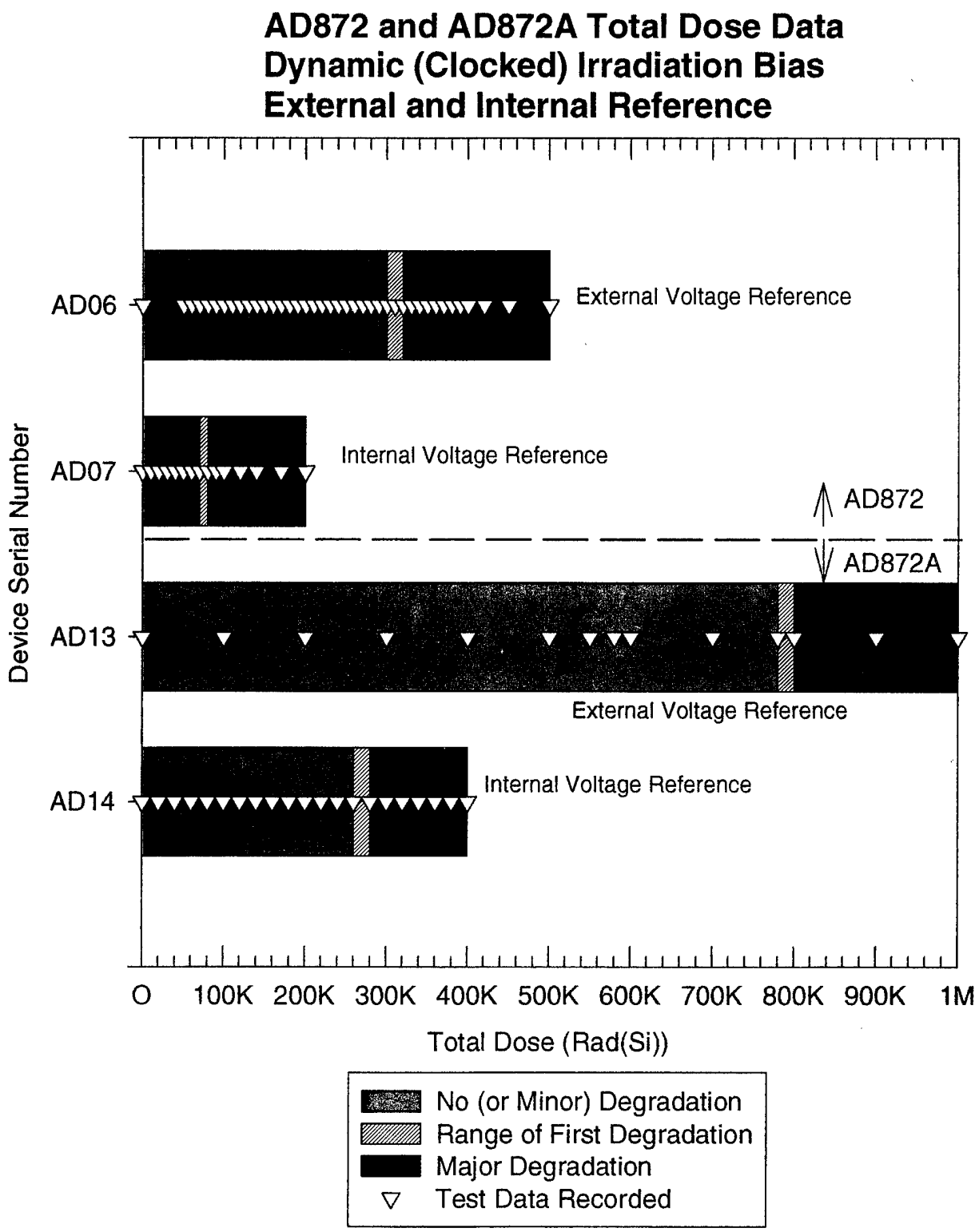

Figure 3. Dynamic Bias Results

Internal Voltage Reference
AD872 & AD872A

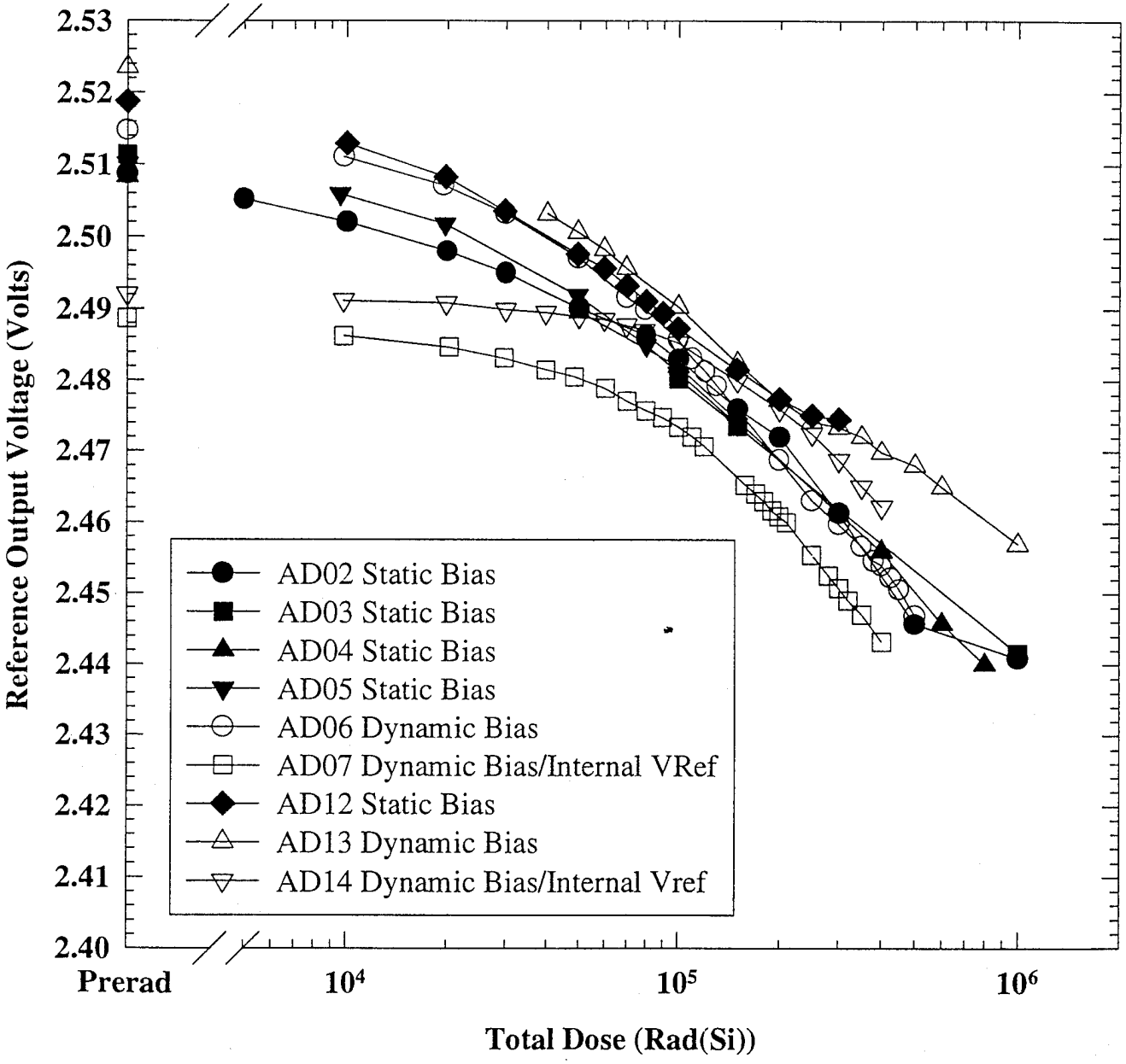

Figure 4. Internal Voltage Reference

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4.5.3 Second Experiment

This second experiment exposed one AD872 and one AD872A using a static bias and external voltage reference, one AD872 and one AD872A using a dynamic bias and external voltage reference and one AD872 and one AD872A using dynamic bias with an internal voltage reference. The exposures of the second experiment were changed from the test plan for the following improvements:

a) To include 3 AD872A parts
b) To minimize annealing by significantly reducing the electrical test time between each radiation interval
c) To check for dependence of the failure level on power supply voltage (add checks at +/- 4.75V and +/- 5.25V)
d) To check radiation performance while using the internal voltage reference
e) To irradiate with a dynamic bias (per original test plan)

As shown by the improved electrical specifications listed in section 1.3.2, the AD872A represents a notable re-design of the AD872. The improved performance can be clearly seen in the pre-irradiation histograms of the two device types shown in Figure 5 (the clusters of spikes in the AD872 data are nearly gone in the AD872A). Since the effect of the circuit changes on device's radiation response were unknown the parts were treated as separate part types during the test. There were 3 AD872's and 3 AD872A's; one part of each type was checked for each of three different bias conditions.

Two changes were made to reduce the time required for electrical tests at each radiation interval. First, the quantity of data taken and recorded was reduced, and second, the data was taken with the part still in the test socket but out of the radiation field. Since it had been demonstrated in the first experiment that functional failure occurred well before parametric failure, the only parametric data recorded was power supply currents, recorded from the bias supplies during exposure (not using the Eagle LSI-5 tester) and the internal voltage reference output voltage. The only functional data collected were histograms, or probability density functions (PDF), taken with the MADCAT system while the part was in the bias socket. To simplify data collection, the four bias supplies, the clock generator, input signal source and a voltmeter connected to the voltage reference were all controlled by computer and this parametric data was continuously recorded at intervals throughout irradiation and functional test. A further advantage of this experimental setup was that during dynamic bias the device could be sampled at any time while the part was in the radiation field. The dose rate was increased to 92.5 rad(Si)/sec. At this dose rate, a 10 KRad(Si) step took 1.8 minutes, while data was collected in just over 30 seconds, compared to about 15 minutes in the first experiment.

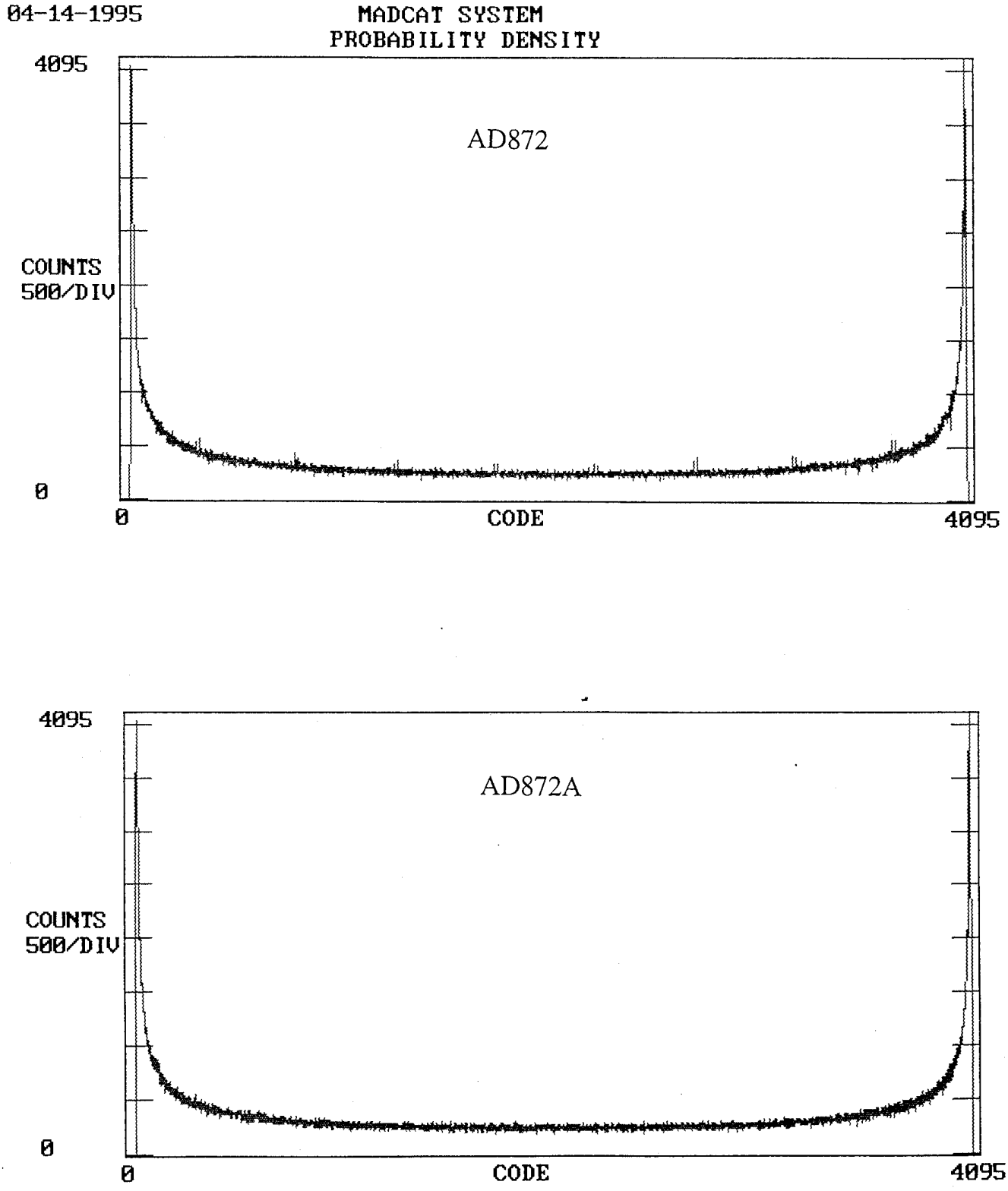


Figure 5. Preirradiation Histograms

Since the first experiment showed less radiation sensitivity with increased power supply voltage, the data was collected at three levels: the minimum rated voltage (+/- 4.75 volts), nominal (+/- 5 volts) and maximum rated voltage (+/-5.25 volts). Collecting data at the two additional voltages only added 10-15 seconds to the test time and characterizes device operation over its operating range.

The original test plan called for testing the three remaining AD872's with a dynamic bias during irradiation. This was modified to accommodate the addition of the three AD872A's to verify data from the first experiment, as well as test parts while using the internal voltage reference. The test equipment used does not reliably collect histogram data at 10 MHz, particularly when used in conjunction with the long cables required. The dynamic tests were all performed with a clock rate of 5 MHz. Previous data on related parts has not shown any significant radiation dependence on clock rate. As discussed, the AD872 and AD872A were treated as different parts for this experiment, which led to three different irradiation bias conditions, with one AD872 and one AD872A tested at each bias:

1) Static Bias (clock and Vin grounded)
2) Dynamic Bias (5 MHz Clock, Vin = 495 kHz, +/- 1 Vp-p)
3) Dynamic Bias with Internal Voltage Reference

The first part tested with a static bias and external voltage reference was an AD872, serial number AD05. Test intervals of 10 KRad(Si) were used. The part passed at all three power supply combinations up to 70 KRad(Si). At 80 KRad(Si), many anomalous counts in the maximum code (4095) were noted at +/- 4.75 volts supply levels. At 100 KRad(Si), the part also failed at nominal supplies. By 110 KRad(Si), failures were observed at all supply levels. Irradiation was completed at 150 KRad(Si). This single datum supports the tentative conclusion of the first experiment that the AD872 is safely usable to about 50 KRad(Si) with a static bias and external reference. The role of annealing in the first experiment has been discussed. AD05s data indicates that annealing did play some role in the data collected on part AD02, but it did not dominate the response, and part-to-part variation in radiation response could be equally large.

An AD872A, serial number AD12, was also tested with a static bias and test intervals of 10 KRad(Si). The design changes made primarily to improve electrical performance and robustness appear to have improved radiation performance quite significantly. No noticeable degradation in the PDF was observed through 240 KRad(Si). At 250 KRad(Si), the shape of the PDF changed significantly, but no missing codes were observed. This was observed at both +/- 4.75 volts and at +/- 5 volts. At 260 KRad(Si), similar degradation was observed at all three supply levels. The device exhibited missing codes at all supply voltages after 270 KRad(Si). Irradiation was completed at 300 KRad(Si). Sample histograms in Figure 6

demonstrate the changes at 250 KRad(Si), and the missing codes at 270 KRad(Si). The observed degradation levels are very high for an unhardened commercial technology. Future tests are being planned on ABCMOS transistors and circuits to understand this data.

Irradiation with a dynamic bias of 5 MHz clock and 495 kHz input signal and an external voltage reference was performed on an AD872, serial number AD06. The part was irradiated to 50 KRad(Si) in a single step, and then tested in 10 KRad(Si) intervals. It was anticipated that radiation performance would improve under dynamic bias. The part passed all tests up to 310 KRad(Si). Between 320 KRad(Si) and 350 KRad(Si) some degradation in the differential non-linearity (DNL) was noted, but the observed changes to the PDF were minor. At 350 KRad(Si), spikes were observed in the PDF, indicating significant degradation. Missing codes were noted at 400 KRad(Si) with a supply bias of +/- 5.25 volts being worst case. Figure 7 demonstrates the data spikes at 350 KRad(Si) and continued degradation at 400 KRad(Si). The PDF degradation pattern with dynamic bias is visibly different from that noted for the static biased AD872's, indicating a different failure mode than observed for static bias. Irradiation was completed at 500 KRad(Si).

A dynamic bias irradiation was performed on an AD872A, serial number AD13. Anticipating relatively high failure thresholds, the test intervals were modified. The part was stepped in 100 KRad(Si) intervals through 300 KRad(Si). From 300 - 800 KRad(Si) data was checked (but not recorded) at 20 KRad(Si) intervals, and recorded at 100 KRad(Si) intervals. As shown in Figure 8, degradation was observed at 800 KRad(Si) at +/- 4.75 volts. By 840 KRad(Si) the part was also degraded at +/- 5 volts. By 880 KRad(Si) degradation was observed at all levels. Irradiation was completed at 1 MRad(Si).

The final bias state used the same dynamic bias as above but changed from an external voltage reference to the internal reference. Since this required modifications to the test board, it was not possible to change back to the external reference to verify differences in performance. The first part irradiated was an AD872, serial number AD07. Again, the part was irradiated in nominal 100 KRad(Si) steps, with data recorded wherever changes were noted, but was checked (with the part in-situ) at 10 KRad(Si) intervals. No change was noticed through 70 KRad(Si), but at 80 KRad(Si), a small, but distinct shift in the range of data collected was noted at +/- 4.75 volts. This requires some explanation: AC functional testing is based upon the expectation that the input signal does not overdrive (or is not clipped by) the ADC. To analyze small changes in performance the signal must not be clipped because the harmonic distortion of the clipped data dominates the response. To this end, the input signal is set to nearly, but not quite full range. Commonly, about 20 bins are allowed at both the top and bottom of the input range (conversely, about 4050 of the 4096 possible bins are utilized during the test). A shift of 5 to 10 bins is visibly noticeable. Such a

shift is what was observed at 80 KRad(Si), and moved the symmetric preirradiation range towards the maximum count of 4095. At this point, the internal reference exhibited a radiation-induced shift from 2.506 volts to 2.474 volts. At 100 KRad(Si), the input range had shifted sufficiently to overdrive the maximum (4095) bin and resulted in low counts in most bins (in this case, the low bin counts are an artifact of the test hardware which stops the test when any bin reaches a 4095 count: this aids in identifying changes in ADC performance). Irradiation continued to 200 KRad(Si) where few non-4095 counts were observed. To verify that the observed failure was caused by the internal reference and not the ADC, the input voltage was reduced from 2.0 volts (peak-to-peak) to 1.8 volts (p-p). The part resumed normal function with this reduced input signal range, and irradiation continued. Continuation of the test served to verify the data taken on part AD06, with dynamic bias and the external voltage reference. Figure 9 displays the data shifted towards the 4095 bins at 100 KRad(Si) and also shows signal degradation within the reduced input range at 350 KRad(Si). The test was concluded at 400 KRad(Si).

The last part tested was a AD872A, serial number AD14. It was irradiated with dynamic bias and the internal voltage reference. The data was recorded at 100 KRad(Si) intervals, with non-recorded checks at 20 KRad(Si) intervals. The first noted change occurred at 280 KRad(Si), where the input range shifted towards the minimum count, or zero bin (compared to a shift towards the maximum count for the AD872). In Figure 10, the 300 KRad(Si) data shows degraded performance at all voltages. Irradiation was completed at 400 KRad(Si). The part resumed functionality at 400 KRad(Si) when the input voltage range was reduced to 1.8 volts (p-p), as shown in Figure 10.

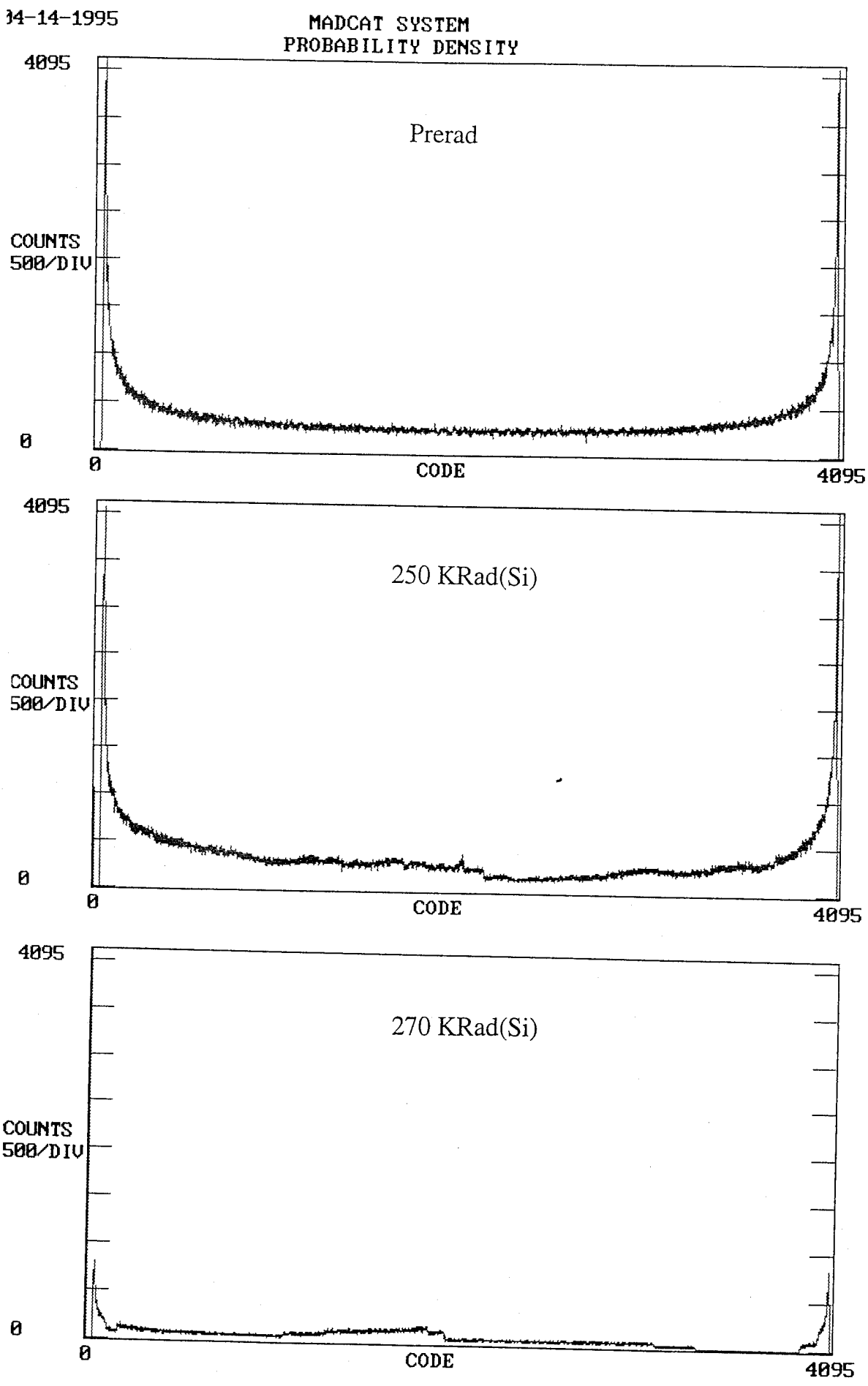


Figure 6. AD12 Histograms

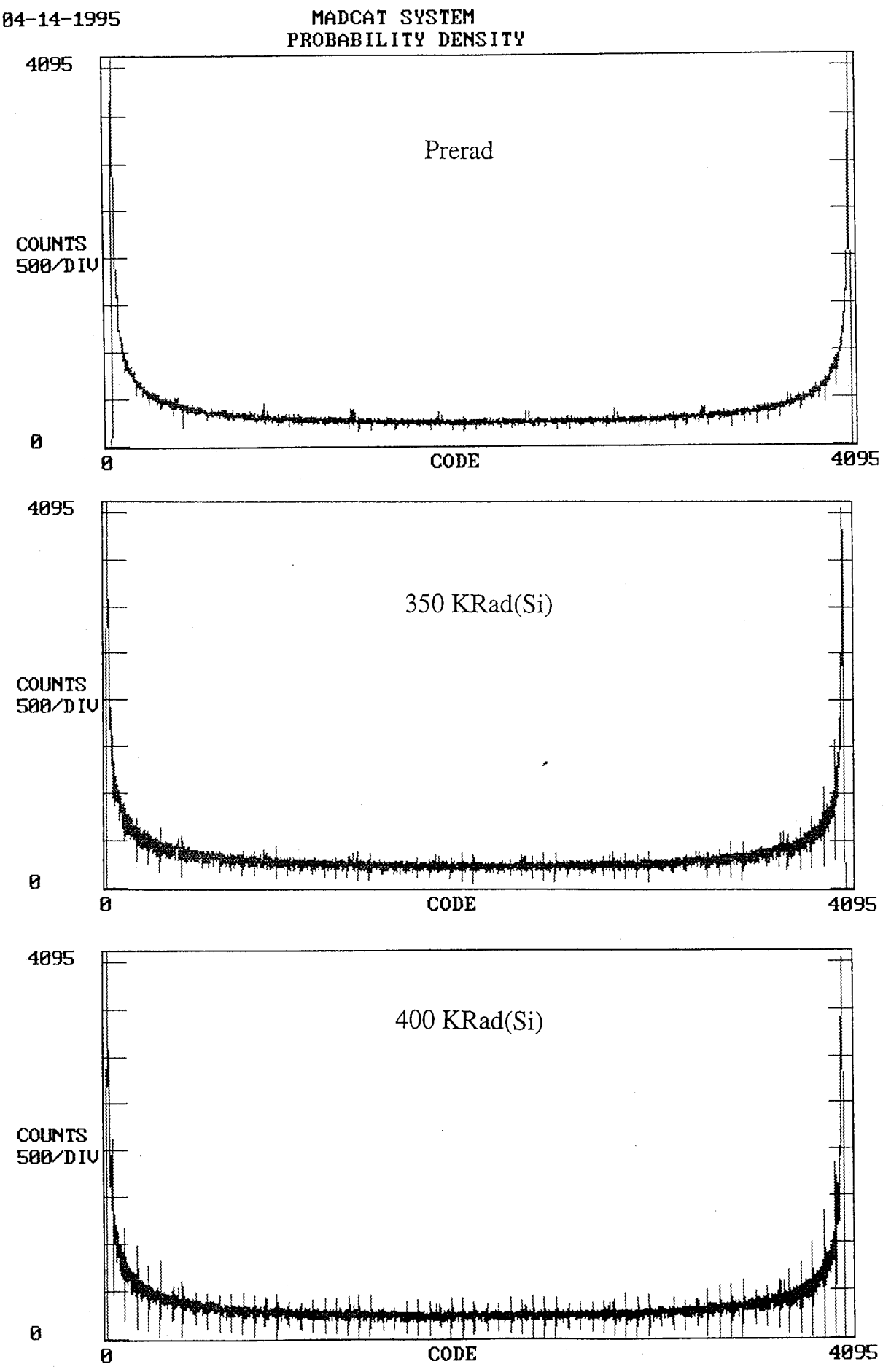


Figure 7. AD06 Histograms

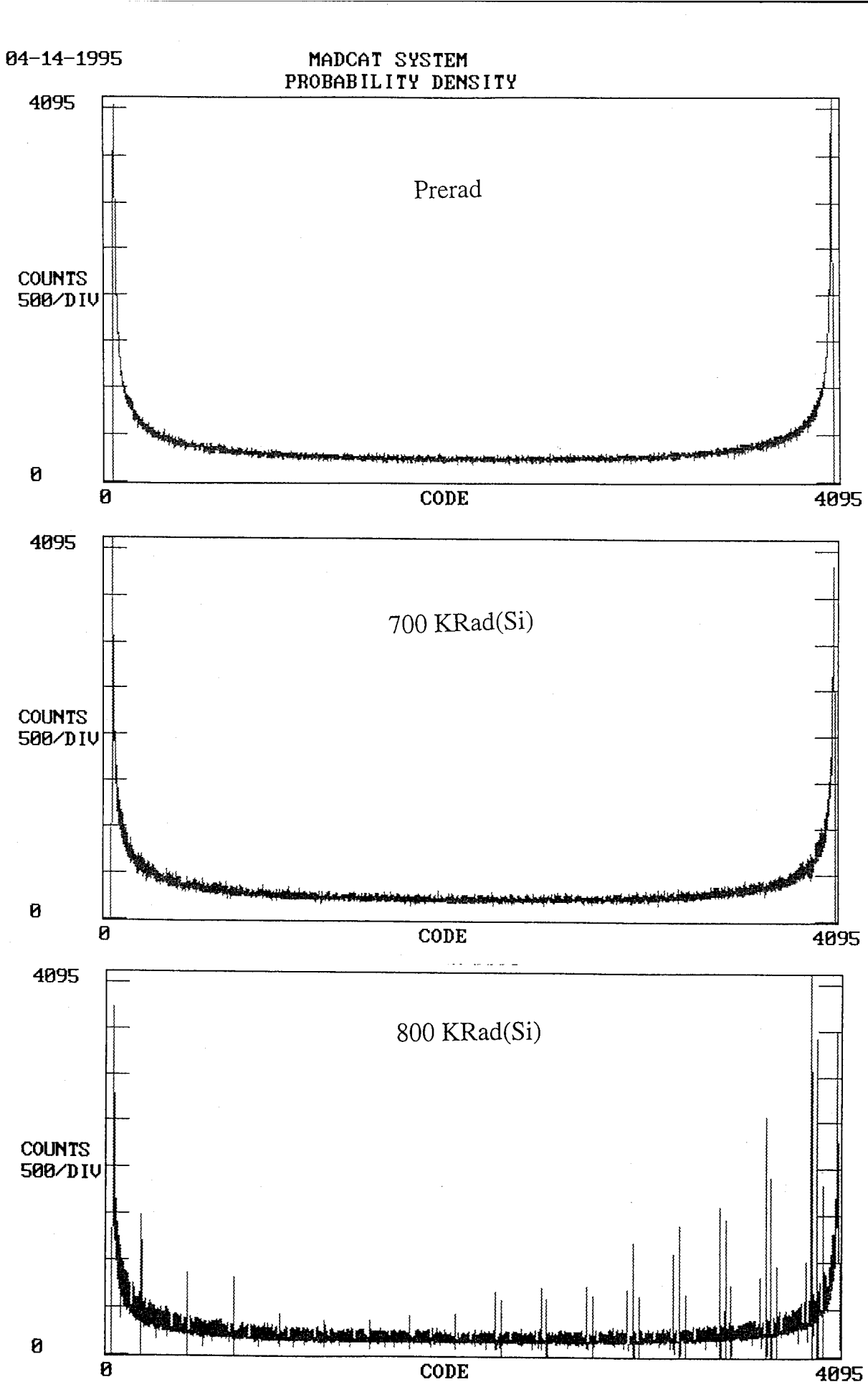


Figure 8. AD13 Histograms

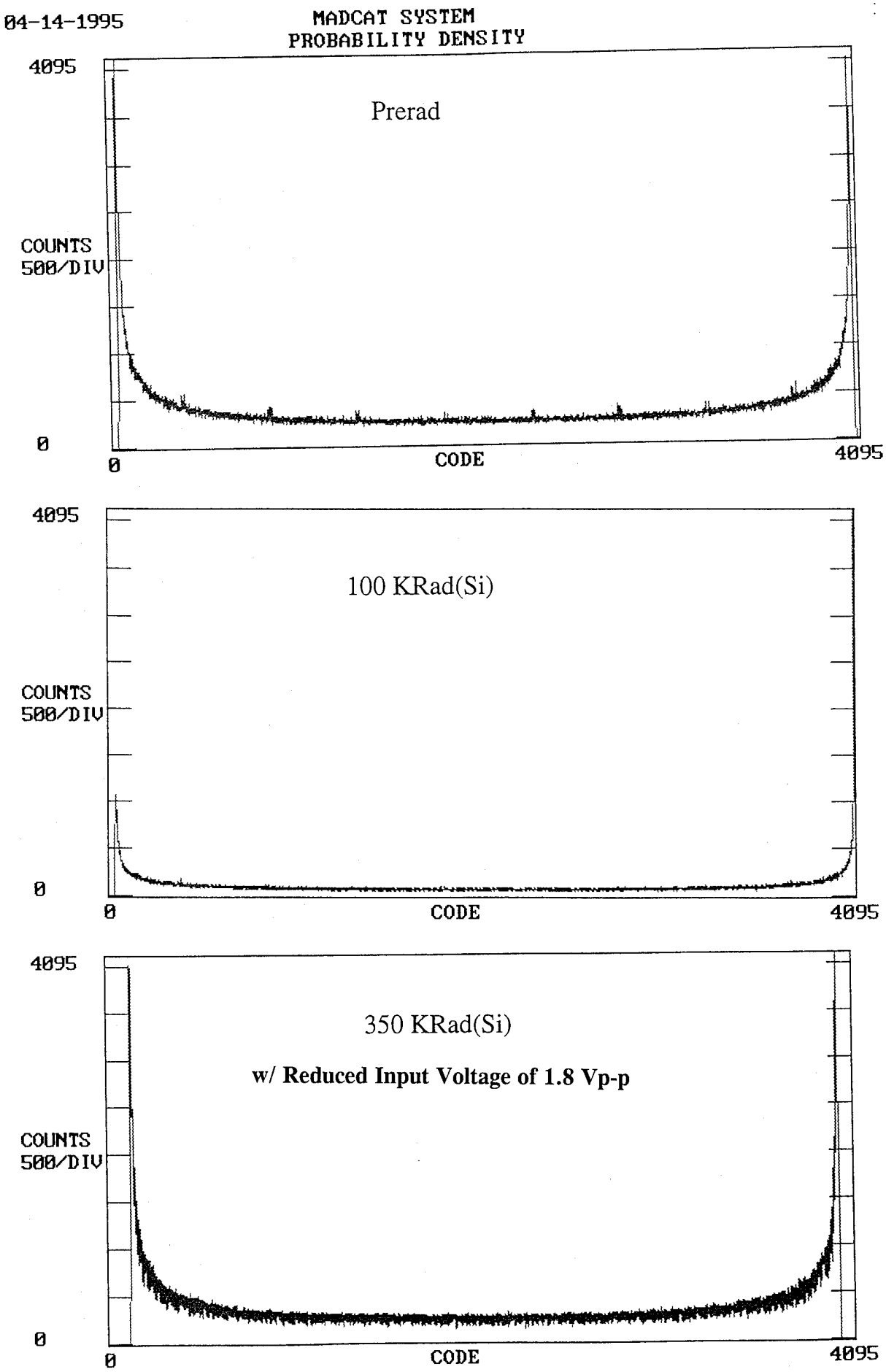


Figure 9. AD07 Histograms/(Using Internal Voltage Reference)

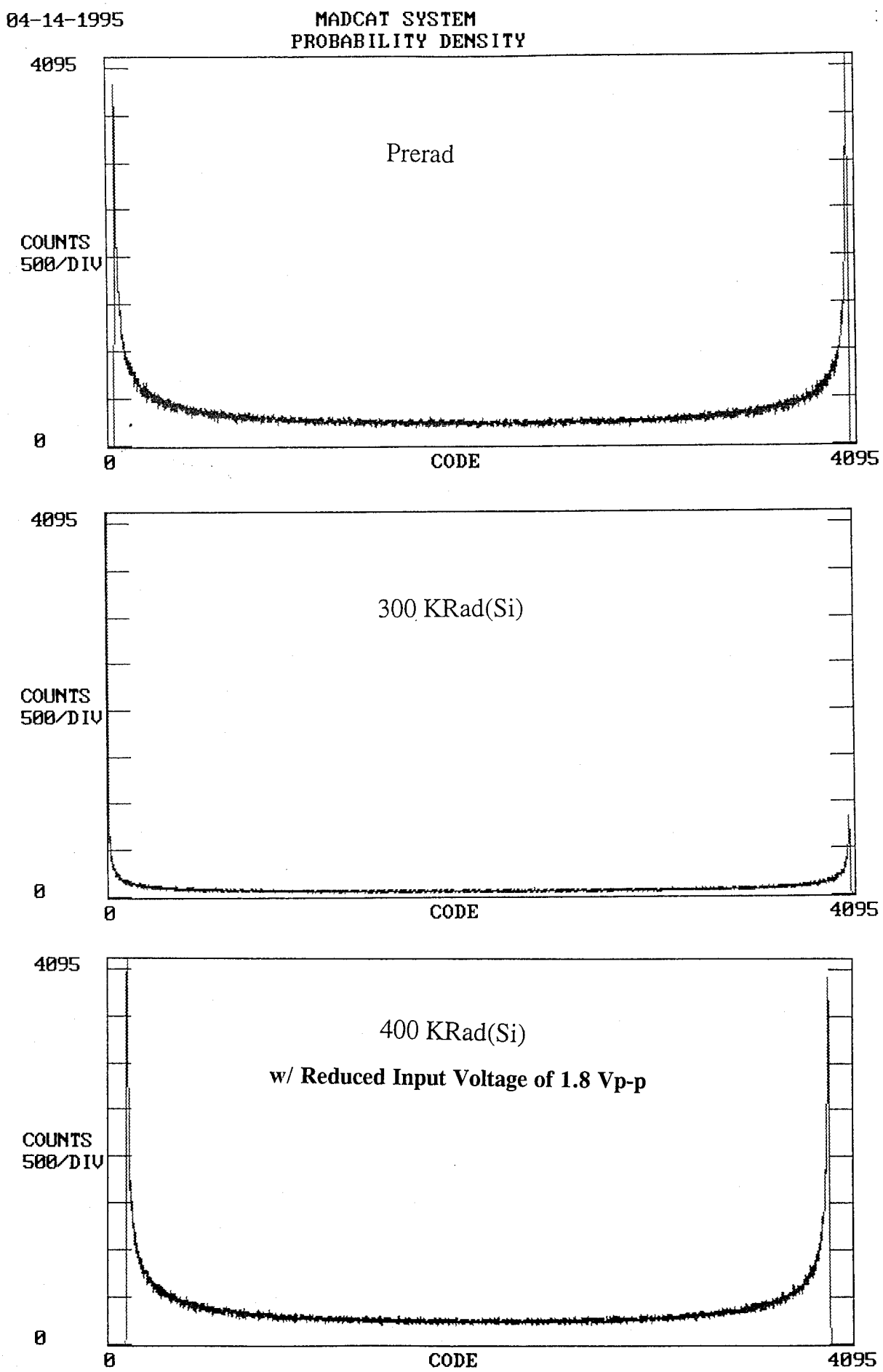


Figure 10. AD14 Histograms/(Using Internal Voltage Reference)

5.0 Dose Rate Test Results

5.1 Test Facility

Four AD872's were tested at the Crane LINAC for upset threshold, total device upset, recovery time, latch-up and survivability. Crane has developed a low-noise, shielded enclosure which was used to test the AD872's. In this configuration, the devices were exposed to 20 ns radiation pulses with dose rates from 3E6 rad(Si)/sec to 1E12 rad(Si)/sec.

5.2 Dosimetry

Primary dosimetry at the Crane LINAC is provided by PIN diode voltage waveforms recorded on digitizers during the pulse. The PIN is reverse biased at 200 volts, and the diode photocurrent discharges a resistor-capacitor network to record the pulse. The area of the pulse is directly proportional to the dose rate of the pulse. The waveform is very consistent with radiation but requires calibration with respect to absolute dose received. This is done with CaF TLDs exposed simultaneously with a recorded waveform. The TLDs require a minimum dose, so multiple pulses are required in some configurations. A calibration routine has been developed at the Crane LINAC which involves a 2-point computer fit between the area of the pulse and the actual dose.

Because a wide range of dose rates were anticipated (1E6 to 1E12 rad(Si)/sec), 2 different PIN diodes were required. The 1N4001 diode is more sensitive than the 6206 diode and works well in the 1E6 to 5E8 rad(Si)/sec range. For higher doses, the 6206 is preferred. The 6206 works over a wide range but must be re-calibrated at high dose rates where the diode saturates (greater than 1E10 rad(Si)/sec). The calibration factors used for the 1N4001 are c1 = 6.7409 and c2 = 0.956. The calibration factors used for the 6202 are c1 = 7.7615 and c2 = 0.922.

For the upset tests done in the 1E6 to 1E10 rad(Si)/sec range, the data was analyzed for consistency and repeatability. An insufficient number of data points were taken at high dose rates to allow similar analysis to be applied above 1E10 rad(Si)/sec). This data is shown in Figure 11-13 as a function of table position versus dose rate. The plots are box plots where, for each position used, the data from 25% to 75% of the mean is displayed as a box. The median is shown as a line through the box. In addition, error bars show the spread of data from the fifth to ninety-fifth percentiles. In Figure 11 the lowest dose rates were achieved using the 4001 diode and a 4 inch aluminum attenuator attached to front of the fixture. The lowest dose rate of about 3E6 rad(Si)/sec, recorded at 50 inches, caused no upsets in any parts. Figure 12 shows the same 1N4001 diode when the aluminum attenuator is removed. The dose rate fixture has a 100 mil aluminum scatter shield which was always used, as was a

lead collimator with a 0.5 inch diameter pass hole. Figure 13 shows the dose rate when the 6206 diode is used in the range from 1E7 to 1E9 rad(Si)/sec.

5.3 Test Procedure

The electrical tests are dynamic in nature with the device clocked at 1 MHz and a DC input voltage. Even though the experimental setup requires cables in excess of 100 feet, a noise floor of less than 4 codes was maintained. The device was irradiated while operating, and the test hardware captures 4096 sequential samples of the ADC output, synchronized with the radiation pulse such that approximately 1000 samples of pre-radiation data are stored, followed by 3000 samples during and after the pulse. The expected converter output is well defined by the DC input voltage so radiation-induced disturbances are apparent. From this data, device functionality, upset and recovery time are deduced. Latch-up and survivability are determined by monitoring the power supply currents in addition to test data.

5.4 Defining ADC Upset

Upset threshold is defined as the dose rate at which a disturbance is detected in the digital data which is greater than the background noise of the test system. In this test, most of the noise was contained within 3 codes, but occasionally 4-6 codes were observed. Upset was recorded when the disturbance in the digital data went above the determined noise floor. Once upset occurs, the magnitude of the upset increases with increasing dose rate until all 12 bits are upset. This level is defined as total device upset.

5.5 Test Results

5.5.1 Upset Threshold and Total Device Upset Results

During the test nearly 200 individual exposures, or tests, were run on the four parts. At each table position (which results in approximately the same dose rate for successive pulses), the device input was set to one of three DC voltages: -0.50 volts, -0.02 volts and +0.50 volts. With an input range of +/- 1 volt, the expected digital output codes are approximately 1000, 2000 and 3000. This checks the device over a wide percentage of its input range. The data shows little variance in upset magnitude with respect to input voltage applied.

In the dose rate range between upset threshold and total device upset the data displays significant variance from point to point, making it difficult to discern the trend of the data. This large variance is believed to result from the relation of the clock edge to the impinging radiation pulse. The tester is not synchronized to the trigger pulse of the LINAC. Assuming the relationship of the clock to the radiation pulse is random,

the data was averaged over small dose rate ranges. The same averaged upset results are displayed in Figures 14 and 15 using two different metrics. The data from the four parts has been averaged over one half decade ranges of dose rate. This interval provided adequate smoothing of the individual sample variance to understand the upset trend.

Figure 14 displays the upset magnitude versus dose rate, where upset magnitude is measured by the number of output codes. For example, if the expected data is code 2000, and the maximum upset level is 2100, then the upset magnitude is 100 codes. The upset threshold of the AD872 is 1E7 rad(Si)/sec, and the total device upset level is about 5E9 rad(Si)/sec. While the upset magnitude displays total device upset well, the upset threshold is not readily observable.

By displaying the upset data in terms of its effective resolution instead of its upset magnitude (Figure 15), the upset threshold is easily observed. Effective Resolution, as defined by equation 1 (for a 12-bit ADC) measures the resolution of the ADC, in bits, after subtracting the portion of its range that has been upset. When no upset exists, the part has an effective resolution of 12-bits. When only 4 output codes are upset, the effective resolution is 10-bits, as the 4 codes of noise are represented by the two least significant bits (lsb). Thus effective resolution is a base 2 logarithmic scale that expresses the resolution of the non-upset portion of the total range of the ADC.

$$\text{Effective Resolution} = \ln(2^{12}/(\text{maxcode-mincode} + 1)/\ln(2) \quad (1)$$

The amplitude of the upset is the number of codes between the minimum code and maximum code, as extracted from the experimental data. As shown in Figure 15, effective resolution displays the small upsets that define upset threshold more effectively than the upset magnitude data of Figure 16, due to its logarithmic nature.

The actual data for the four devices is displayed in Figures 16-19.

5.5.2 Recovery Time

Recovery time measurements were calculated for every shot. The recovery time for all four parts was less than 10μsec up to 1E10 Rad(Si)/sec and less than 1msec for a dose rate of 8E11 Rad(Si)/sec.

5.5.3 Latch-up

Latch-up is detected by either a sustained increase in power supply current or by loss of functionality. It is usually a temporary condition, recoverable by cycling device power. Latch-up may also lead to permanent damage by destruction of metallization

or transistors from the heavy current induced by the latch condition. The AD872's did not latch under any condition tested, up to a dose rate of 1E12 rad(Si)/sec.

5.5.4 Survivability

Survivability is the ability of the device to survive a given radiation level without permanent damage from the radiation. The AD872's survived all tests without damage up to a dose rate of 1E12 rad(Si)/sec.

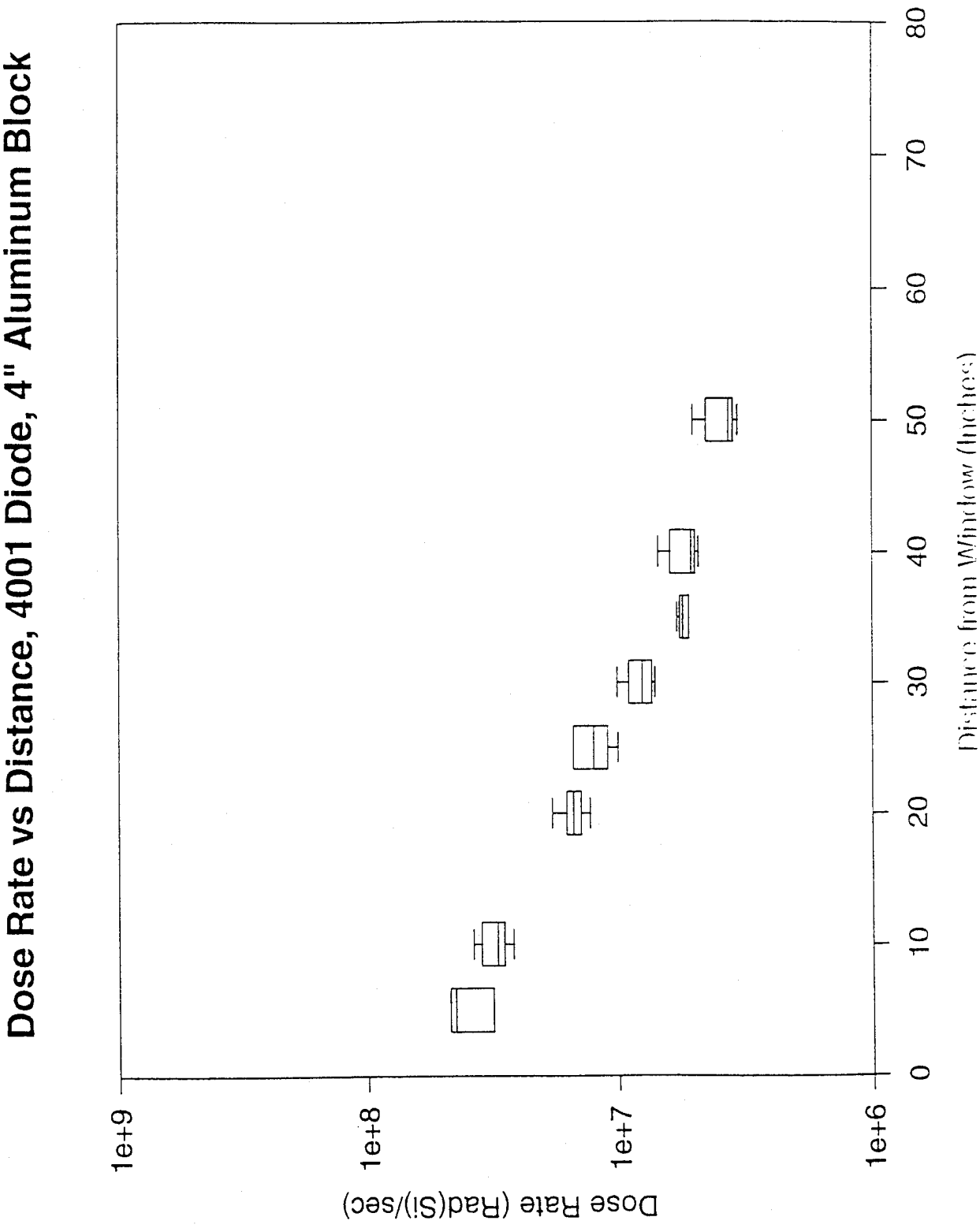


Figure 11. 1N4001 Diode Dosimetry/With Aluminum Block

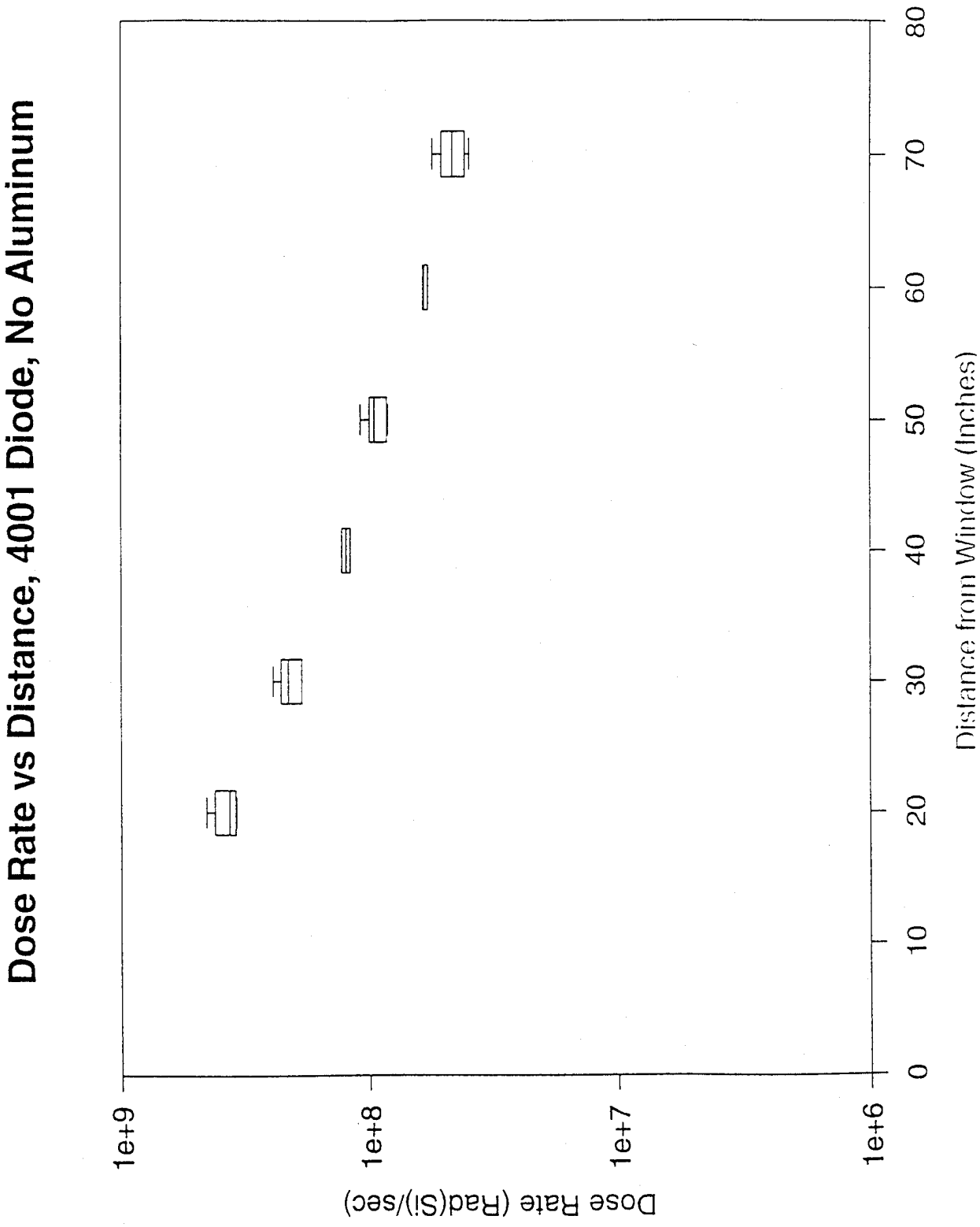


Figure 12. 1N4001 Diode Dosimetry/No Auminum Block

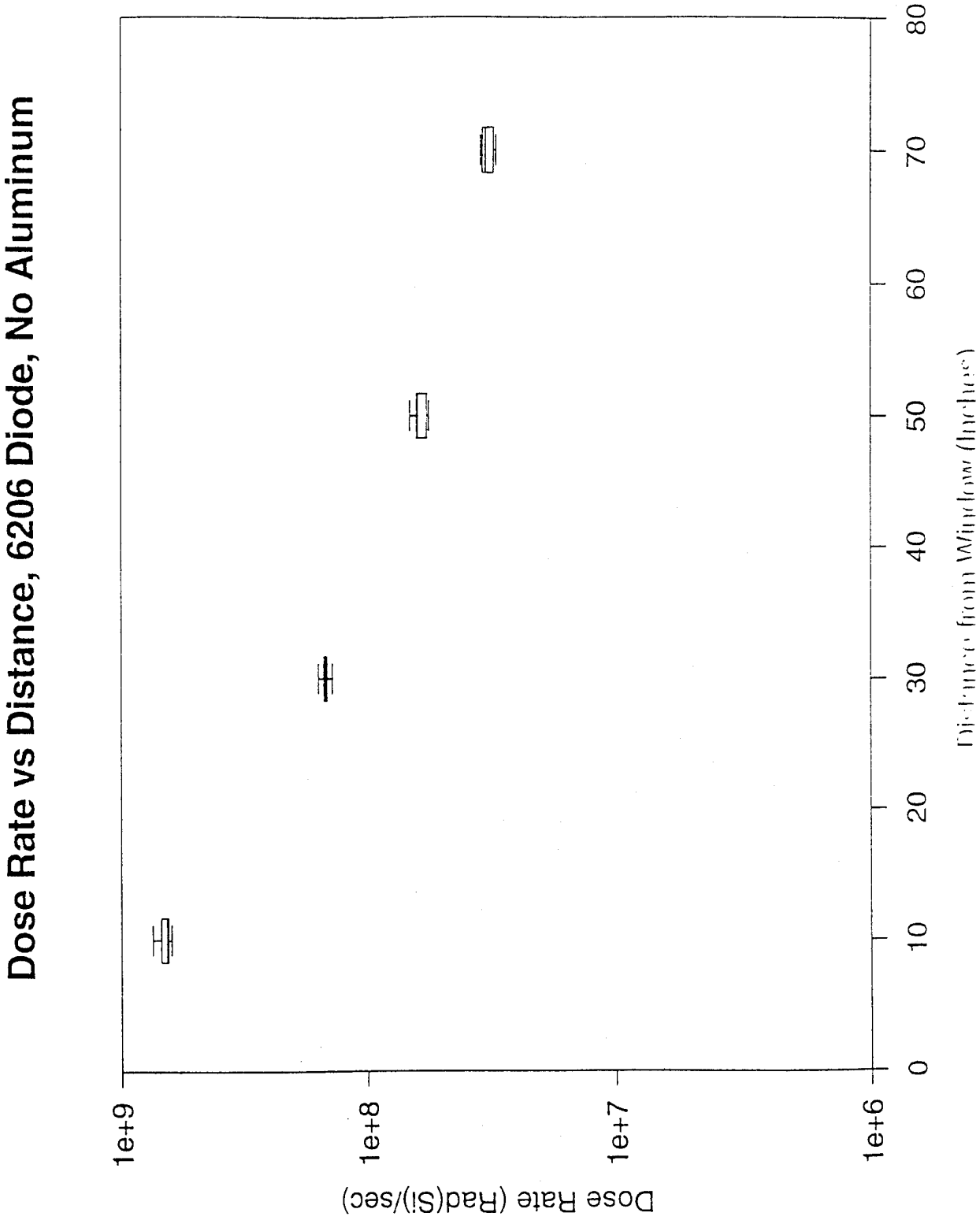


Figure 13. 6202 Diode Dosimetry/No Aluminum Block

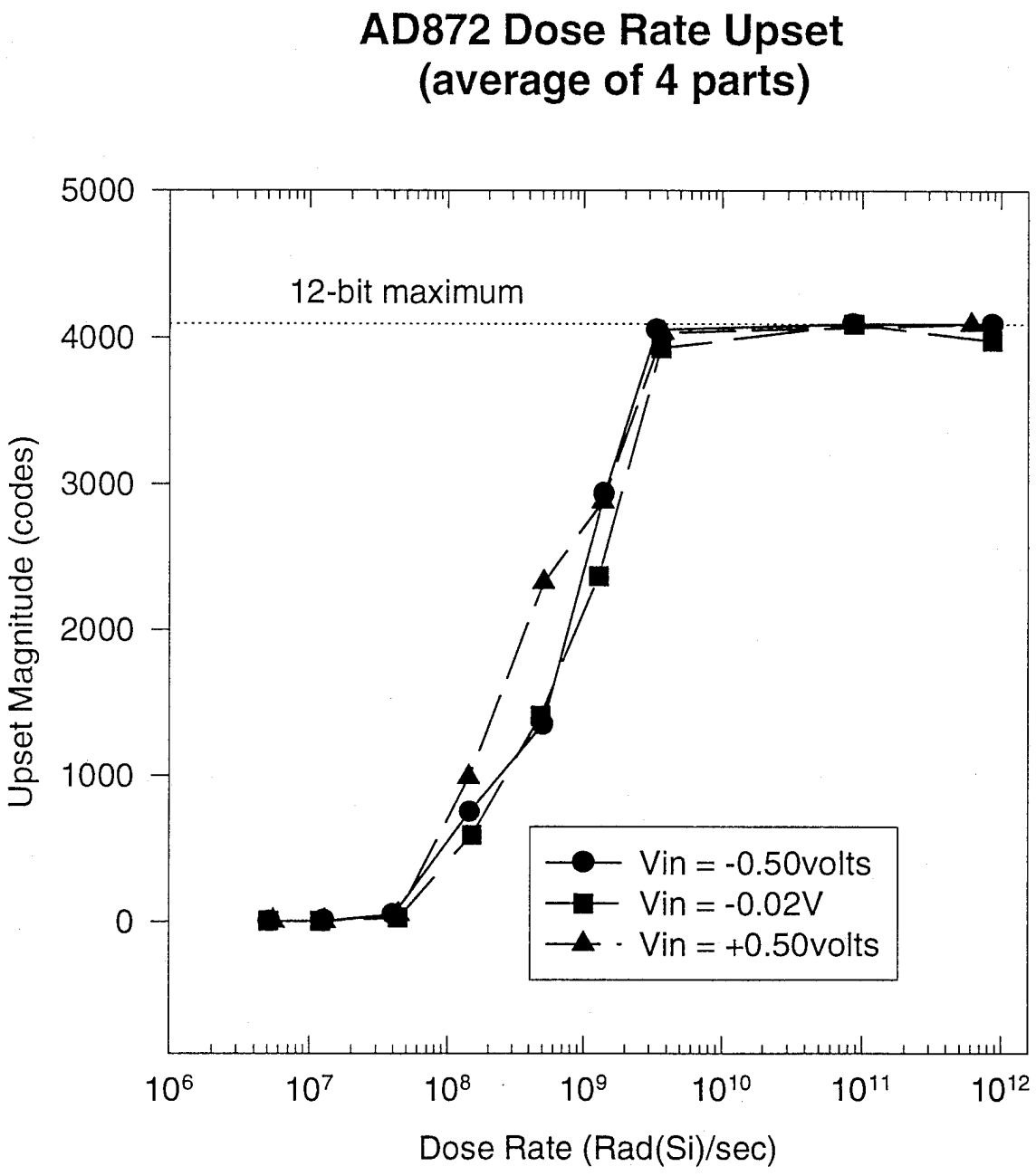


Figure 14. Upset Magnitude versus Dose Rate

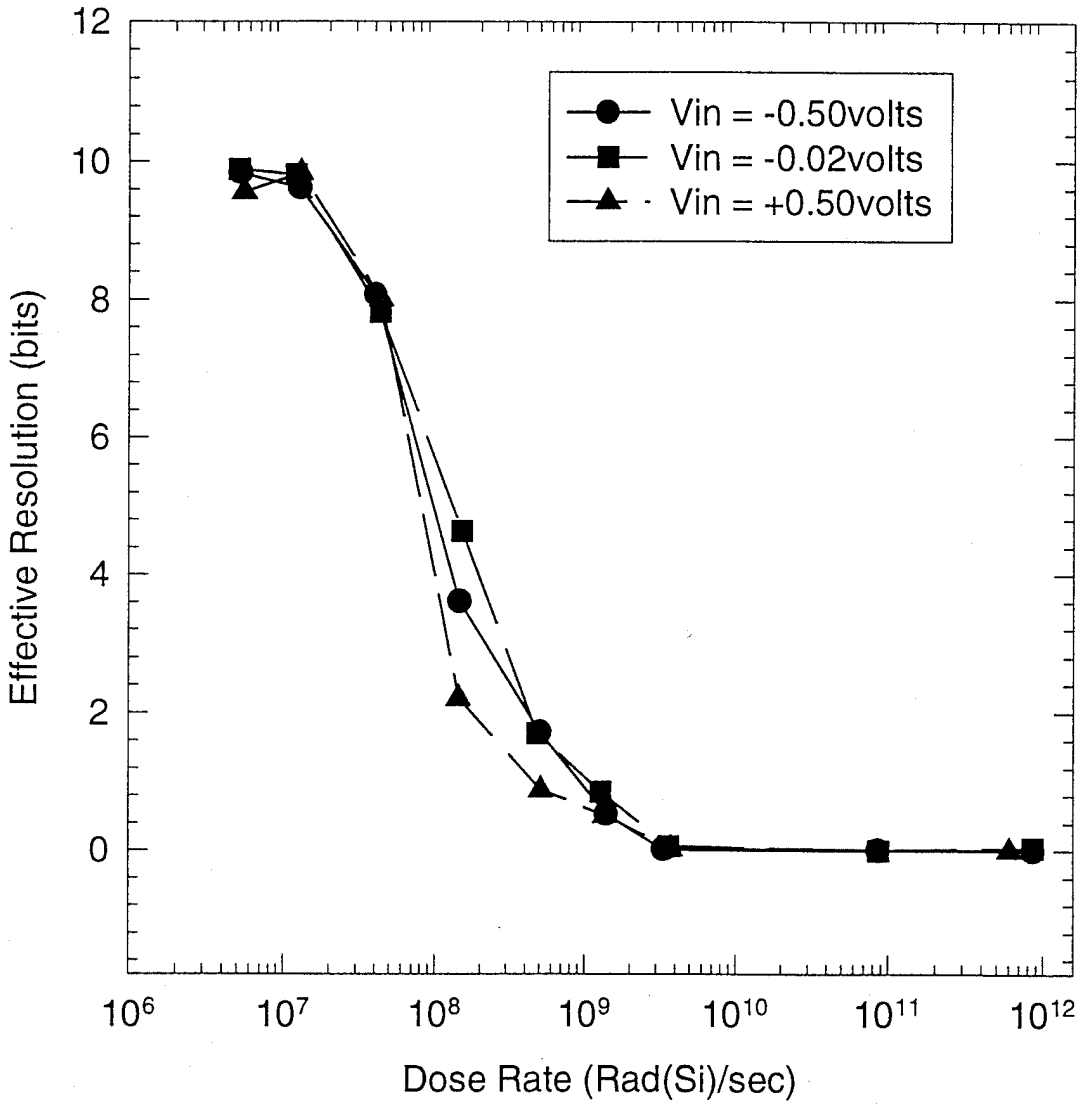


Figure 15. Effective Resolution versus Dose Rate

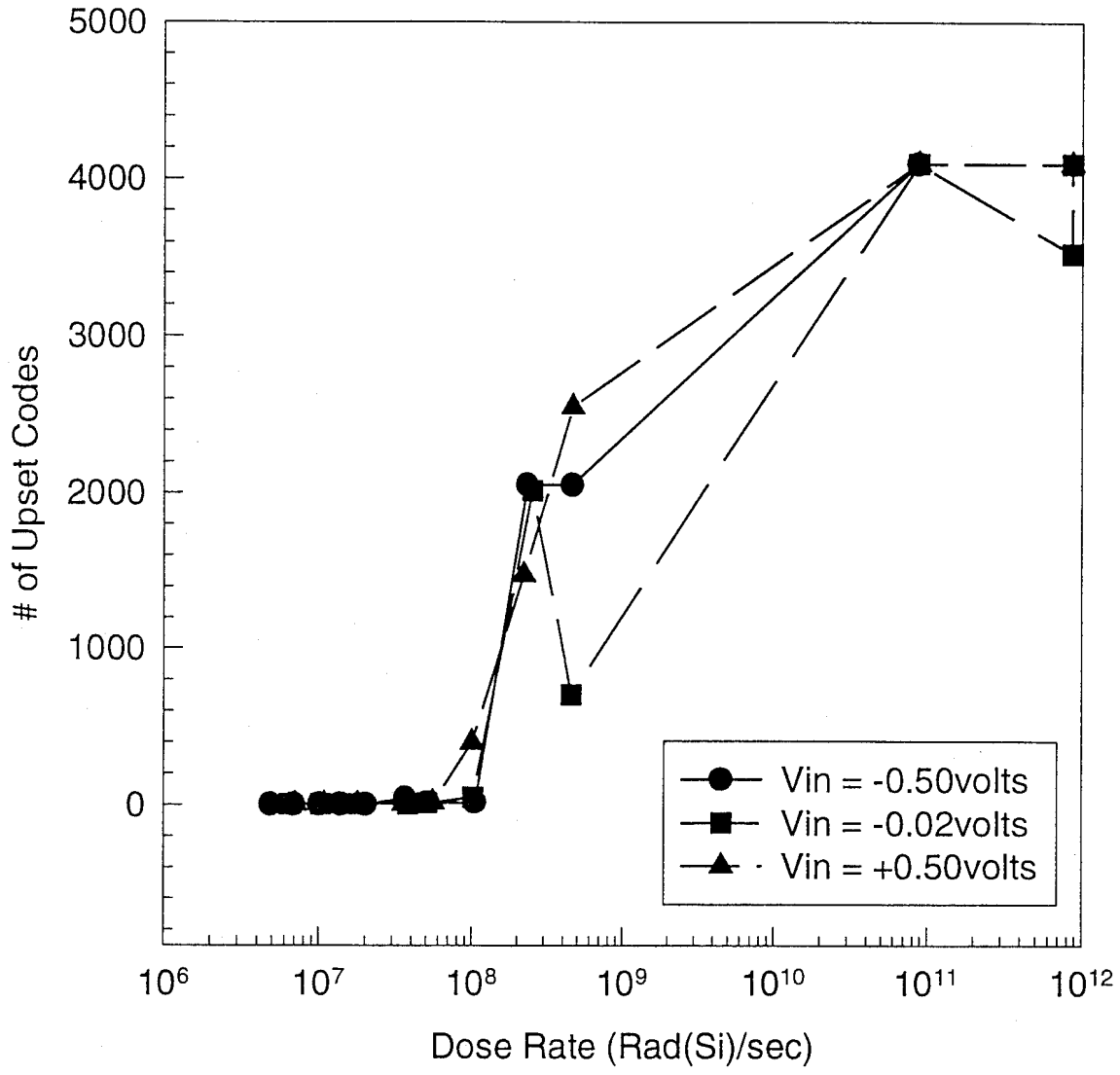


Figure 16. AD08

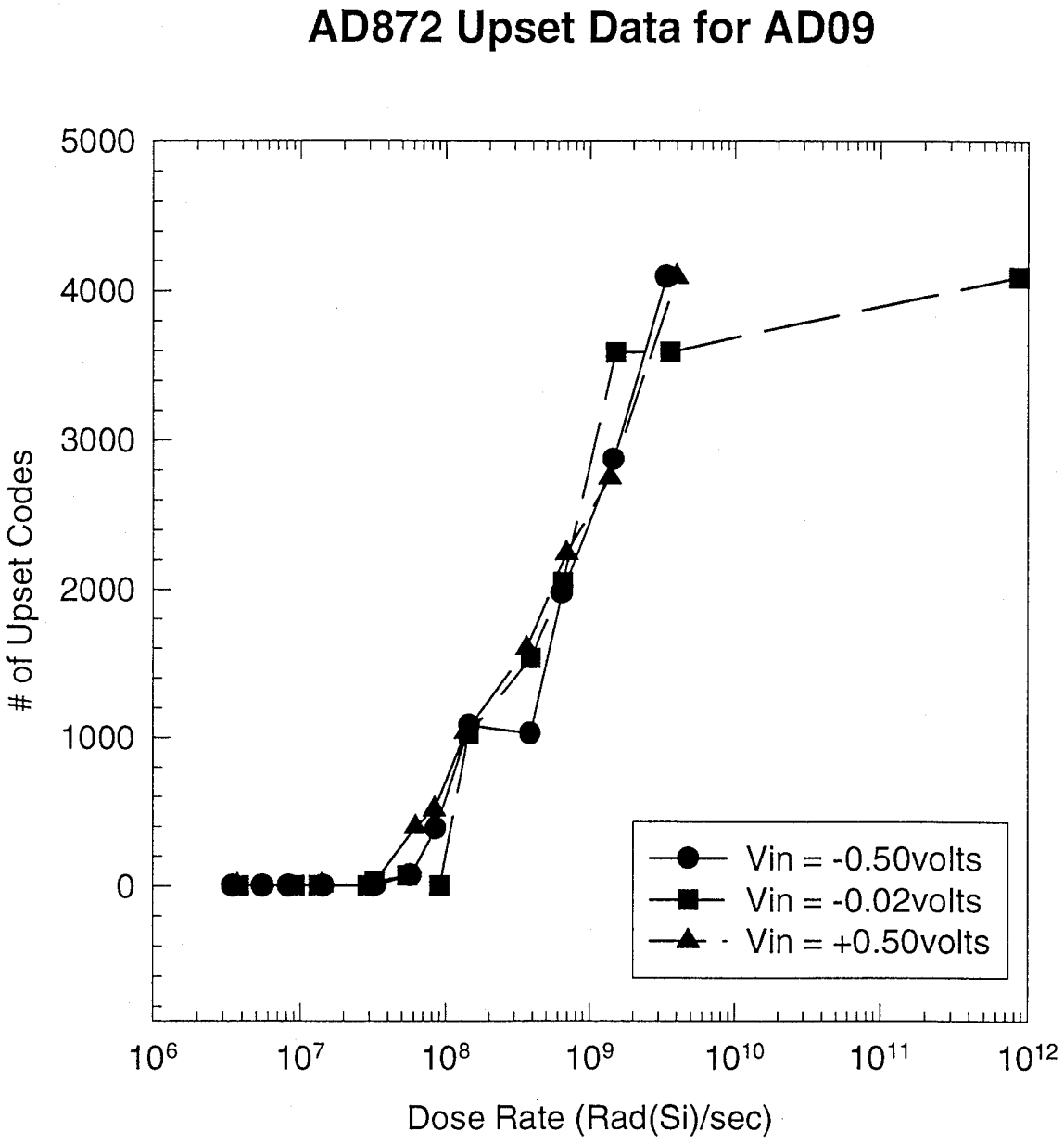


Figure 17. AD09

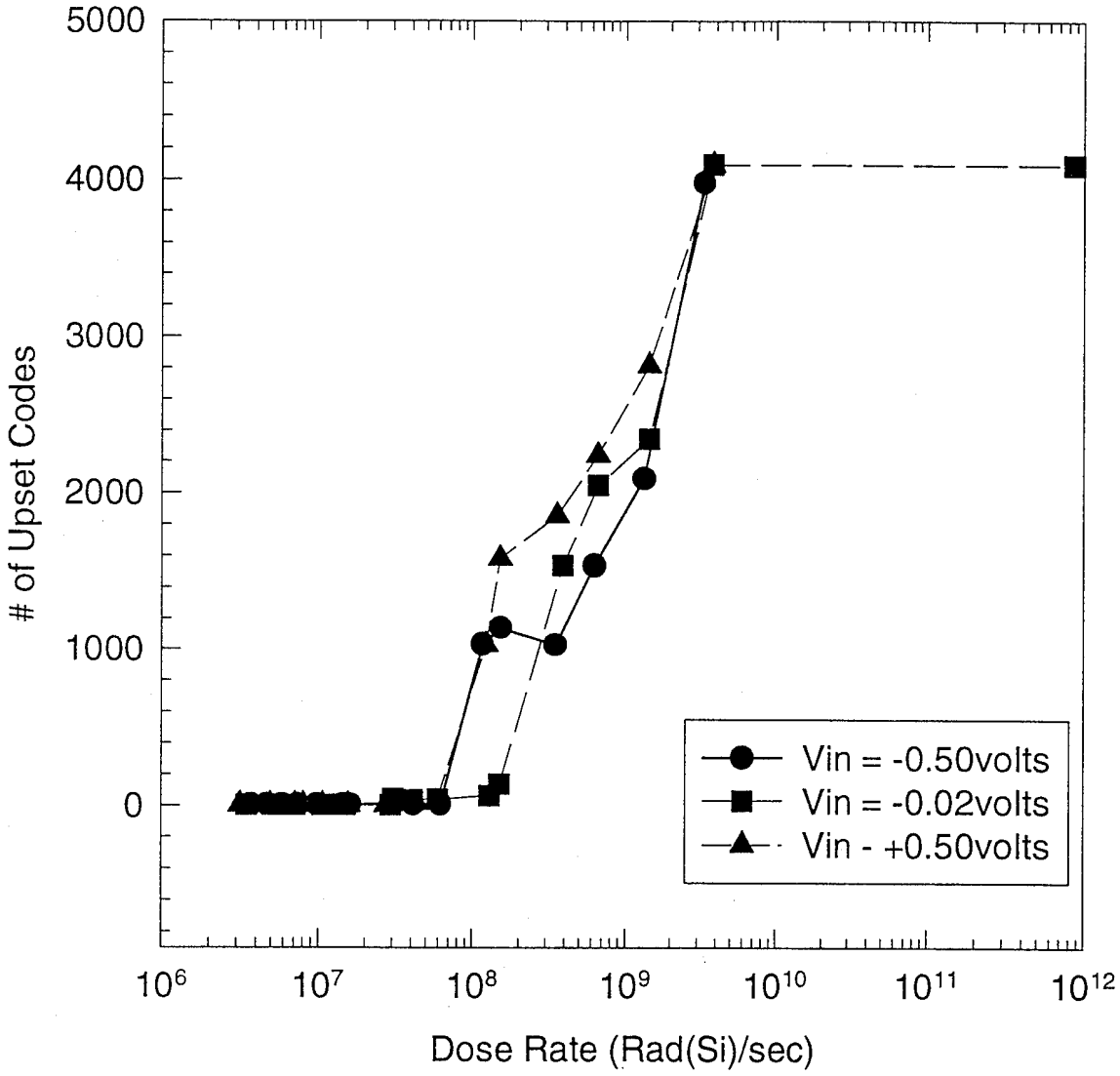


Figure 18. AD10

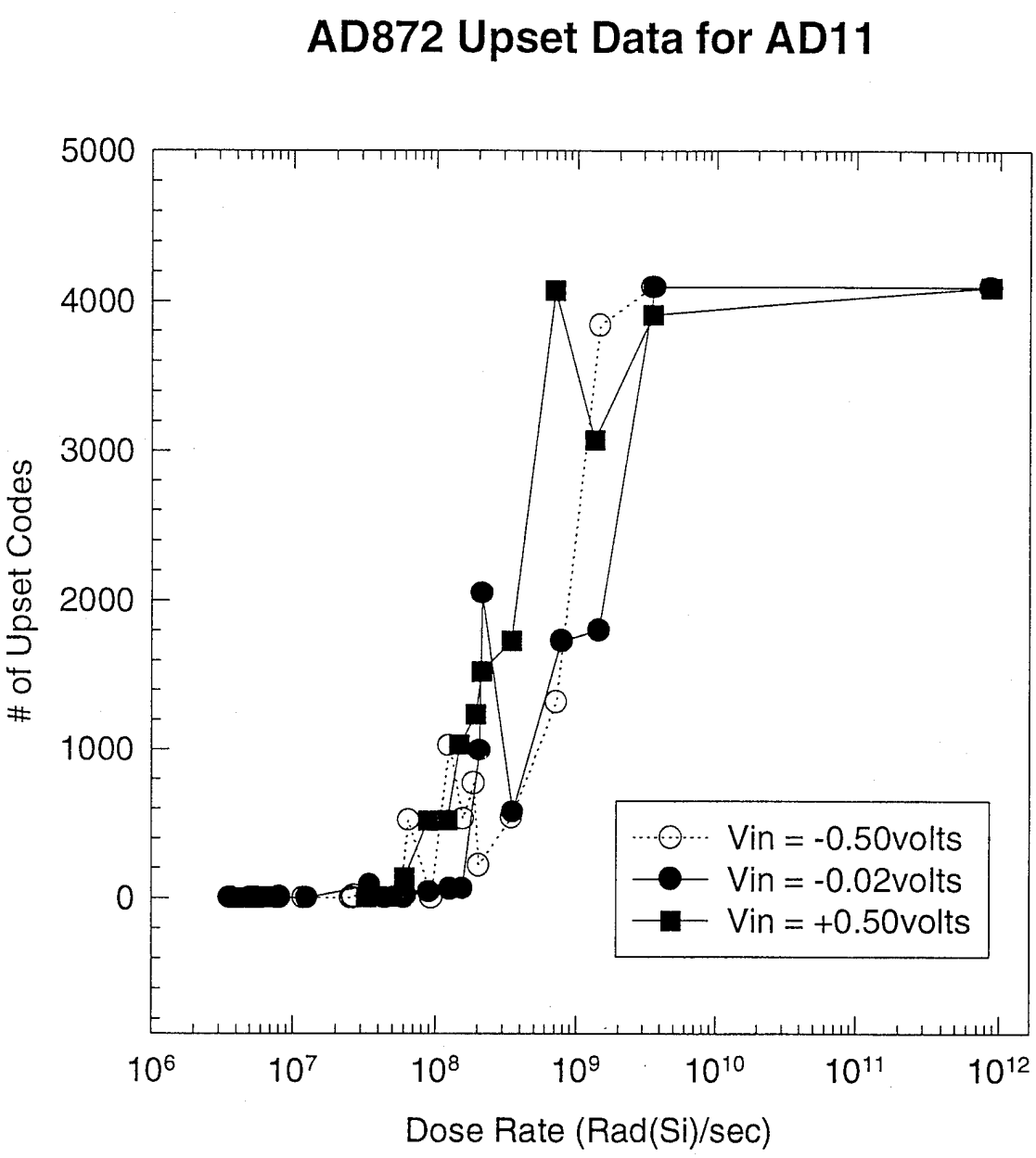


Figure 19. AD11

6.0 Conclusions and Recommendations

Both the AD872 and AD872A appear to be excellent candidate parts for systems with moderate radiation requirements. The small sample size of this test does not allow confidence in the potential range of radiation response of a large population of these devices, but a conservative estimate of worst case performance would conclude the AD872 is usable, with an external reference, to 50 KRad(Si). The AD872A should be usable in excess of 100 KRad(Si), again with an external reference. Periodic review of radiation performance will be required for system use, as the commercial ABCMOS process is not maintained for radiation performance. For a given application with very stringent requirements on device dynamic performance, the degradation criteria used in this test may not suffice. For such criteria, degradation levels may be lower than reported.

The AD872 also displayed excellent dose rate performance. No latch-up or survivability problems were observed up to a dose rate of 1E12 rad(Si)/sec. The upset threshold is 1E7 rad(Si)/sec, and the total device upset level is about 5E9 rad(Si)/sec.

The performance of both device types exceeded initial expectations for a commercial technology. It is recommended that additional AD872A's from several date codes be tested to verify the reported performance. In addition, ABCMOS test transistors should be tested to characterize the technology. Finally, the AD872A devices should be checked in the dose rate environment prior to system selection. While significant change is not anticipated, the significant circuit and layout changes require the part be revisited.

APPENDIX A:

Test Plan

APPENDIX A: TEST PLAN

1. TEST DEVICES: NSWC Crane has received 11 AD872A commercial ADC. These parts are fabricated in the commercial ABCMOS process, which is not radiation-hardened. Limited testing was done on this process at Crane about 4 years ago, but the process has been refined since that time. These tests indicate that the parts will probably exhibit functional and parametric failure after exposure to 10-20 KRad(Si). Latch-up is possible, given the bulk substrate, but this part shares basic layout with the radiation-hardened AD9872, and has a better chance of not latching than most commercial devices.

2. TOTAL DOSE FACILITY: The total dose experiment will be performed in the NSWC Shepherd Model 81-22 Cobalt-60 Irradiator, with tunnel model 484, located in Building 2088. The test fixture will be enclosed in a lead-aluminum box to shield low-energy x-rays. The test will conform to test method 1019.4. The planned dose rate is 50-60 Rad(Si)/sec, which is at the low end of the range allowed by 1019.4. This is used to increase the accuracy of the small radiation steps required by a relatively soft part.. Dosimetry will be done using Thermoluminesent Dosimetry. The TLDs will be read at the Crane TLD reader in Building 3059.

3. DOSE RATE FACILITY: The dose rate experiment will be performed at the NSWC Linac, located in Building 3059. The test boards will be mounted in a shielded enclosure used for low noise tests. In this configuration, dose rates can range from less than 1E7 Rad(Si)/sec to greater than 1E12 Rad(Si)/sec. Dosimetry is primarily from a PIN diode mounted in the fixture. The PIN is calibrated to TLDs on a regular basis.

4. TEST MATRIX: Of the 11 parts, 6 will be exposed to total dose, 4 to dose rate, and 1 will be held as a test standard. Previous test on similar parts has shown a static bias condition to be worst case for total dose exposure, but dynamic bias simulates operational conditions. The test matrix follows:

Number	Test Type	Clock	Input Condition
3	TD Static	GND	GND
3	TD Dynamic	10 MHz	Sine Wave, 991 KHz,Full Scale
4	DR Dynamic	1 MHz	DC, 0.45V, 0.01V, -0.75V

5. ELECTRICAL TESTS: Prior to irradiation, and at each total dose exposure interval, all parts will be electrically tested, for parametric data, and dynamic performance. Parametric parameters tested will include power supply currents, analog

input voltage range, Vol, Voh, Iol, Ioh, and internal reference voltage. Dynamic tests (performed with an external reference voltage) will include Fast-Fourier Transform of 4K data samples to establish Signal-to-Noise Ratio (SNR) and Effective Number Of Bits (ENOB), and Probability Density Function (PDF) to establish Integral and Differential Non-Linearity (INL, DNL). The pre-irradiation tests will be performed in an optimized fixture, which is very low noise. Dose rate tests are done in-situ, with longer cable runs than optimum. For these tests there will be some small degradation of performance, usually only 2-3 dB in SNR. This does not create any problems as degradation is measured relative to the in-fixture pre-irradiation values.

6. TOTAL DOSE TEST: Since the parts are anticipated to be relatively soft, the first part will be a static bias device, and will be tested in 5 kRad(Si) steps. Based upon the results of this test, the step-stress intervals may be adjusted to improve resolution of the threshold. The test will be repeated until failure. The dynamic tests will monitor power supply currents, but will not measure dynamic performance in-situ. All dynamic tests will be done with the parts removed from the irradiation fixture, to the laboratory fixture.

7. DOSE RATE TEST: The dose rate tests will characterize the devices for upset threshold, total device upset threshold, recovery time, latch-up and survivability. Both latch-up and survivability are checked primarily by monitoring the power supply currents, but also by checking for continued functionality of the device. Latch-up is monitored during all tests, but survivability requires the part to be exposed to much larger dose rates than will be required to achieve total device upset. Assuming no latch-up, the parts will be survivability tested to a maximum dose rate of 1E12 Rad(Si)/sec. Upset and recovery time are measured dynamically by collecting 4096 sequential samples of ADC output data. The Linac is triggered after approximately 1000 samples of pre-irradiation data have been collected. In previous tests, the noise floor for this configuration has been just below 3-bits, so first upset occurs when bit upset occurs at a magnitude greater than 3-bits. Upset threshold, total device upset threshold and recovery time are all extracted from effective resolution data. The effective resolution of the device, as defined by the equation 1, will be plotted versus dose rate:

$$\text{Effective Resolution} = \ln(212/(\text{max-min} + 1)/\ln(2) \text{ bits} \qquad (1)$$

The amplitude of the upset is the number of bits between the minimum code and maximum code (max-min), as taken from the experimental data. Recovery time is measured as the time from the first detectable upset sample, until the device has returned to pre-irradiation conditions. Total dose accumulation will be monitored to prevent any part from being tested after it exceeds one half of its expected failure level. This may limit

the amount of survivability data taken, as the parts are relatively soft. High dose rate data will be collected after upset data is completed.

8. TEST REPORTING: Preliminary data will be made available to PMA-A1151 within a few days of the test. It will consist of viewfoils that summarize initial findings. A complete technical report will be delivered to PMA-A1151 for distribution approximately 3 weeks after the test is completed. Based upon the current schedule, this will be 14 April 1995.

APPENDIX B:

AD872A Electrical Specification

12/12/94

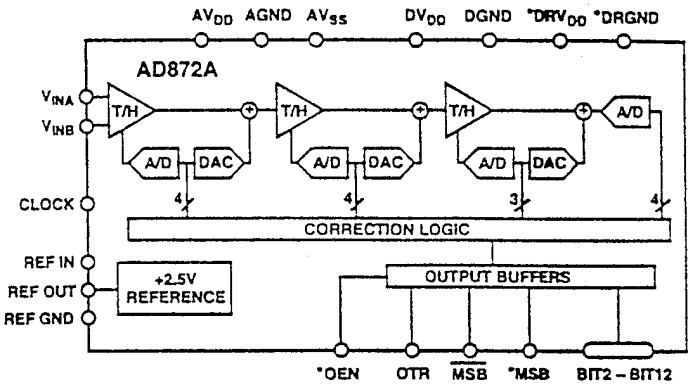
Complete 12-Bit 10 MSPS Monolithic A/D Converter

AD872A

FEATURES

Monolithic 12-Bit 10 MSPS A/D Converter
Low Noise: 0.26 LSB RMS Referred-to-Input
No Missing Codes Guaranteed
Differential Nonlinearity Error: 0.5 LSB
Signal-to-Noise and Distortion Ratio: 68 dB
Spurious-Free Dynamic Range: 75 dB
Power Dissipation: 1.03 W
Complete: On-Chip Track-and-Hold Amplifier and Voltage Reference
Twos Complement Binary Output Data
Out-of-Range Indicator
28-Pin Ceramic DIP or 44-Pin Surface Mount Package

FUNCTIONAL BLOCK DIAGRAM



*ONLY AVAILABLE ON 44-PIN SURFACE MOUNT PACKAGE

PRODUCT DESCRIPTION

The AD872A is a monolithic 12-bit, 10 Msps analog-to-digital converter with an on-chip, high performance track-and-hold amplifier and voltage reference. The AD872A uses a multistage differential pipelined architecture with error correction logic to provide 12-bit accuracy at 10 Msps data rates and guarantees no missing codes over the full operating temperature range. The AD872A is a redesigned version of the the AD872 which has been optimized for lower noise. The AD872A is pin compatible with the AD872, allowing the parts to be used interchangeably as system requirements change.

The low noise input track-and-hold (T/H) of the AD872A is ideally suited for high-end imaging applications. In addition, the T/H's high input impedance and fast settling characteristics allow the AD872A to easily interface with multiplexed systems that switch multiple signals through a single A/D converter. The dynamic performance of the T/H also renders the AD872A suitable for sampling single channel inputs at frequencies up to and beyond the Nyquist rate. The AD872A provides both reference output and reference input pins, allowing the on-board reference to serve as a system reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. A single clock input is used to control all internal conversion cycles. The digital output data is presented in twos complement binary output format. An out-of-range signal indicates an overflow condition, and can be used with the most significant bit to determine low or high overflow.

The AD872A is fabricated on Analog Devices' ABCMOS-1 process that utilizes high speed bipolar and CMOS transistors on a single chip.

The AD872A is packaged in a 28-pin ceramic DIP and a 44-pin leadless ceramic surface mount package (LCC). Operation is specified from 0°C to +70°C and –55°C to +125°C.

PRODUCT HIGHLIGHTS

The AD872A offers a complete single-chip sampling, 12-bit 10 Msps analog-to-digital conversion function in a 28-pin DIP or 44-pin LCC.

Low Noise—The AD872A features 0.26 LSB rms referred to-input noise.

Low Power—The AD872A at 1.03 W consumes a fraction of the power of presently available hybrids.

On-Chip Track-and-Hold (T/H)—The low noise, high impedance T/H input eliminates the need for external buffers and can be configured for single-ended or differential inputs.

Ease of Use—The AD872A is complete with T/H and voltage reference and is pin-compatible with the AD872.

Out of Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD872A's input range.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD872A–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AV_{DD} = + 5 V, DV_{DD} = +5 V, AV_{SS} = –5 V, f_{SAMPLE} = 10 MHz unless otherwise noted)

Parameter	J Grade[1]	S Grade[1]	Units
RESOLUTION	12	12	Bits min
MAX CONVERSION RATE	10	10	MHz min
INPUT REFERRED NOISE	0.26	0.26	LSB rms typ
ACCURACY			
Integral Nonlinearity (INL)	±1.75	±1.75	LSB typ
Differential Nonlinearity (DNL)	±0.5	±0.5	LSB typ
No Missing Codes	12	12	Bits Guaranteed
Zero Error (@ +25°C)[2]	±0.75	±0.75	% FSR max
Gain Error (@ +25°C)[2]	±1.25	±1.25	% FSR max
TEMPERATURE DRIFT			
Zero Error	±0.15	±0.3	% FSR max
Gain Error[3, 4]	±0.80	±1.75	% FSR max
Gain Error[3, 5]	±0.25	±0.50	% FSR max
POWER SUPPLY REJECTION[6]			
AV_{DD}, DV_{DD} (+5 V ± 0.25 V)	±0.125	±0.125	% FSR max
AV_{SS} (–5 V ± 0.25 V)	±0.125	±0.125	% FSR max
ANALOG INPUT			
Input Range	±1.0	±1.0	V max
Input Resistance	50	50	kΩ typ
Input Capacitance	10	10	pF typ
INTERNAL VOLTAGE REFERENCE			
Output Voltage	2.5	2.5	V typ
Output Voltage Tolerance	±20	±40	mV max
Output Current (Available for External Loads) (External Load Should Not Change During Conversion)	2.0	2.0	mA typ
REFERENCE INPUT RESISTANCE	5	5	kΩ
POWER SUPPLIES			
Supply Voltages			
AV_{DD}	+5	+5	V (±5% AV_{DD} Operating)
AV_{SS}	–5	–5	V (±5% AV_{SS} Operating)
DV_{DD}	+5	+5	V (±5% DV_{DD} Operating)
DRV_{DD}[7]	+5	+5	V (±5% DRV_{DD} Operating)
Supply Current			
IAV_{DD}	91	92	mA max (85 mA typ)
IAV_{SS}	147	150	mA max (115 mA typ)
IDV_{DD}	20	21	mA max (7 mA typ)
$IDRV_{DD}$[7]	2	2	mA
POWER CONSUMPTION	1.03 1.25	1.03 1.3	W typ W max

NOTES

[1]Temperature ranges are as follows: J Grade: 0°C to +70°C, S Grade: –55°C to +125°C.

[2]Adjustable to zero with external potentiometers (see Zero and Gain Error Calibration section).

[3]+25°C to T_{MIN} and +25°C to T_{MAX}.

[4]Includes internal voltage reference drift.

[5]Excludes internal voltage reference drift.

[6]Change in Gain Error as a function of the dc supply voltage ($V_{NOMINAL}$ to V_{MIN}, $V_{NOMINAL}$ to V_{MAX}).

[7]LCC package only.

Specifications subject to change without notice.

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, AV_{DD} = + 5 V, DV_{DD} = +5 V, AV_{SS} = –5 V, f_{SAMPLE} = 10 MHz unless otherwise noted)[1]

Parameter	J Grade	S Grade	Units
SIGNAL-TO-NOISE & DISTORTION RATIO (S/N+D)			
f_{INPUT} = 1 MHz	68	68	dB typ
	61	61	dB min
f_{INPUT} = 4.99 MHz	66	66	dB typ
SIGNAL-TO-NOISE RATIO (SNR)			
f_{INPUT} = 1 MHz	69	69	dB typ
f_{INPUT} = 4.99 MHz	67	67	dB typ
TOTAL HARMONIC DISTORTION (THD)			
f_{INPUT} = 1 MHz	–74	–74	dB typ
	–63	–62	dB max
f_{INPUT} = 4.99 MHz	–72	–72	dB typ
SPURIOUS-FREE DYNAMIC RANGE (SFDR)			
f_{INPUT} = 1 MHz	75	75	dB typ
f_{INPUT} = 4.99 MHz	74	74	dB typ
INTERMODULATION DISTORTION (IMD)[2]			
Second Order Products	–80	–80	dB typ
Third Order Products	–73	–73	dB typ
FULL POWER BANDWIDTH	35	35	MHz typ
SMALL SIGNAL BANDWIDTH	35	35	MHz typ
APERTURE DELAY	6	6	ns typ
APERTURE JITTER	16	16	ps rms typ
ACQUISITION TO FULL-SCALE STEP	40	40	ns typ
OVERVOLTAGE RECOVERY TIME	40	40	ns typ

NOTES

[1] f_{INPUT} amplitude = –0.5 dB full scale unless otherwise indicated. All measurements referred to a 0 dB (1.0 V pk) input signal unless otherwise indicated.

[2] fa = 1.0 MHz, fb = 0.95 MHz with t_{SAMPLE} = 10 MHz.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AV_{DD} = + 5 V, DV_{DD} = +5 V, AV_{SS} = –5 V, f_{SAMPLE} = 10 MHz unless otherwise noted)

Parameter	Symbol	J, S Grades	Units
LOGIC INPUTS			
High Level Input Voltage	V_{IH}	+2.0	V min
Low Level Input Voltage	V_{IL}	+0.8	V max
High Level Input Current (V_{IN} = DV_{DD})	I_{IH}	±10	µA max
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	±10	µA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUT			
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	+2.4	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	+0.4	V max
Output Capacitance	C_{OUT}	5	pF typ
Leakage (Three State, LCC Only)	IZ	±10	µA max

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, AV_{SS} = −5 V; V_{IL} = 0.8 V, V_{IN} = 2.0 V, V_{OL} = 0.4 V and V_{OH} = 2.4 V)

Parameter	Symbol	J, S Grades	Units
Clock Period[1]	t_C	100	ns min
CLOCK Pulse Width High	t_{CH}	45	ns min
CLOCK Pulse Width Low	t_{CL}	45	ns min
Clock Duty Cycle[2]		40	% min (50% typ)
		60	% max
Output Delay	t_{OD}	10	ns min (20 ns typ)
Pipeline Delay (Latency)		3	Clock Cycles
Data Access Time (LCC Package Only)[2]	t_{DD}	50	ns typ (100 pF Load)
Output Float Delay (LCC Package Only)[2]	t_{HL}	50	ns typ (10 pF Load)

NOTES
[1]Conversion rate is operational down to 10 kHz without degradation in specified performance.
[2]See section on Three-State Outputs for timing diagrams and applications information.
Specifications subject to change without notice.

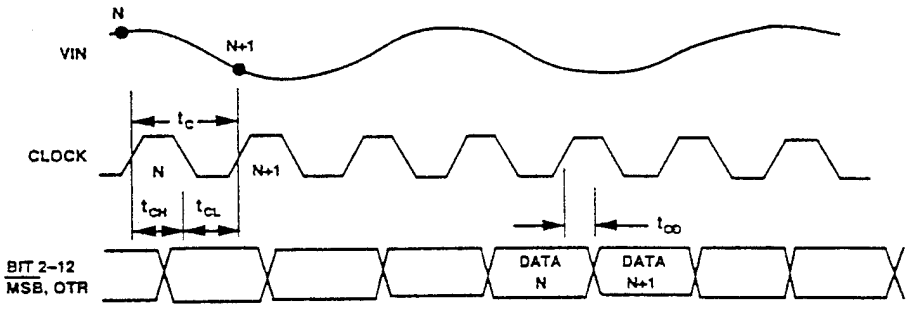


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	With Respect to	Min	Max	Units
AV_{DD}	AGND	−0.5	+6.5	Volts
AV_{SS}	AGND	−6.5	+0.5	Volts
DV_{DD}, DRV_{DD}[2]	DGND, DRGND[2]	−0.5	+6.5	Volts
DRV_{DD}[2]	DV_{DD}	−6.5	+6.5	Volts
DRGND	DGND	−0.3	+0.3	Volts
AGND	DGND	−1.0	+1.0	Volts
AV_{DD}	DV_{DD}	−6.5	+6.5	Volts
Clock Input, OEN[2]	DGND	−0.5	DV_{DD} + 0.5	Volts
Digital Outputs	DGND	−0.5	DV_{DD} + 0.3	Volts
V_{INA}, V_{INB}, REF IN	AGND	−6.5	+6.5	Volts
REF IN	AGND	AV_{SS}	AV_{DD}	Volts
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
[2]LCC package only.

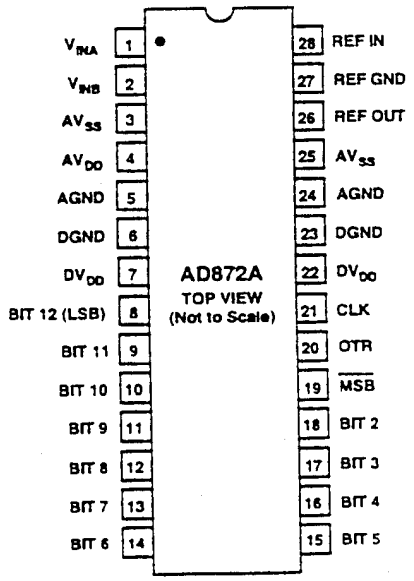
PIN DESCRIPTION

Symbol	DIP Pin No.	LCC Pin No.	Type	Name and Function
AGND	5, 24	9, 36	P	Analog Ground.
AV_{DD}	4	6, 38	P	+5 V Analog Supply.
AV_{SS}	3, 25	5, 40	P	–5 V Analog Supply.
$\overline{MSB}$	19	29	DO	Inverted Most Significant Bit. Provides twos complement output data format.
MSB	N/A	27	DO	Most Significant Bit.
BIT 2–BIT 11	18–9	26–17	DO	Data Bits 2 through 11.
BIT 12 (LSB)	8	16	DO	Least Significant Bit.
CLK	21	31	DI	Clock Input. The AD872A will initiate a conversion on the rising edge of the clock input. See the Timing Diagram for details.
DV_{DD}	7, 22	33	P	+5 V Digital Supply.
DGND	6, 23	10	P	Digital Ground.
DRV_{DD}	N/A	12, 32	P	+5 V Digital Supply for the output drivers.
DRGND	N/A	11, 34	P	Digital Ground for the output drivers. (See section on Power Supply Decoupling for details on DRV_{DD} and DRGND.)
OTR	20	30	DO	Out of Range is Active HIGH on the leading edge of Code 0 or the trailing edge of Code 4096. See Output Data Format Table III.
OEN	N/A	13	DI	Output Enable. See the Three State Output Timing Diagram for details.
REF GND	27	42	AI	Reference Ground.
REF IN	28	43	AI	Reference Input. +2.5 V input gives ±1 V full-scale range.
REF OUT	26	41	AO	+2.5 V Reference Output. Tie to REF IN for normal operation.
V_{INA}	1	1	AI	(+) Analog Input Signal on the differential input amplifier.
V_{INB}	2	2	AI	(–) Analog Input Signal on the differential input amplifier.
NC	N/A	3, 4, 7, 8, 14, 15, 28, 35, 37, 39, 44		No Connect.

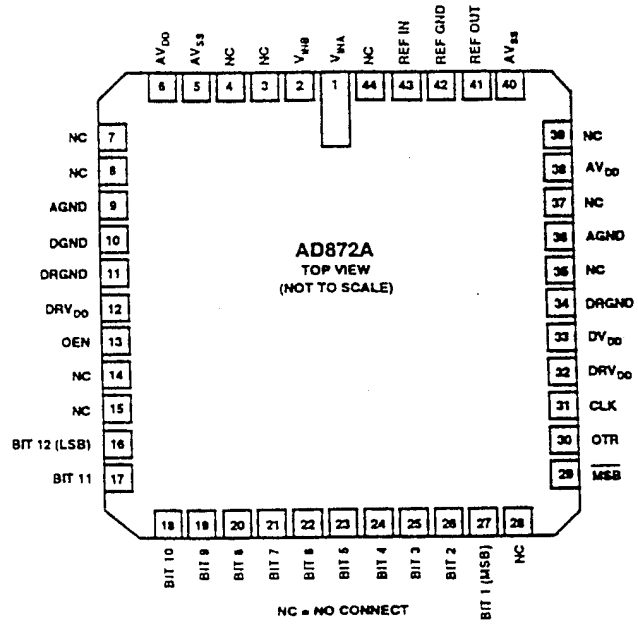
TYPE: AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; P = Power; N/A = Not Available on 28-pin DIP. Only available on 44-pin surface mount package.

PIN CONFIGURATIONS

28-Pin Ceramic DIP



44-Pin LCC



DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR (INL)
Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL LINEARITY ERROR (DNL, NO MISSING CODES)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes must be present over all operating ranges.

ZERO ERROR
The major carry transition should occur for an analog value 1/2 LSB below analog common. Zero error is defined as the deviation of the actual transition from that point. The zero error and temperature drift specify the initial deviation and maximum change in the zero error over temperature.

GAIN ERROR
The first code transition should occur for an analog value 1/2 LSB above nominal negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TEMPERATURE DRIFT
The temperature drift for zero error and gain error specifies the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION
The specifications show the maximum change in the converter's full scale as the supplies are varied from nominal to min/max values.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

APERTURE DELAY
Aperture delay is a measure of the Track-and-Hold Amplifier (THA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

OVERVOLTAGE RECOVERY TIME
Overvoltage recovery time is defined as that amount of time required for the ADC to achieve a specified accuracy after an overvoltage (50% greater than full-scale range), measured from the time the overvoltage signal reenters the converter's range.

DYNAMIC SPECIFICATIONS
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa – fb), and the third order terms are (2 fa + fb), (2 fa – fb), (fa + 2 fb) and (2 fb – fa). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is –0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

FULL-POWER BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

SPURIOUS FREE DYNAMIC RANGE
The difference, in dB, between the rms amplitude of the input signal and the peak spurious signal.

ORDERING GUIDE

Model	Temperature Range	Package Option[1]
AD872AJD	0°C to +70°C	D-28
AD872AJE	0°C to +70°C	E-44A
AD872ASD[2]	–55°C to +125°C	D-28
AD872ASE[2]	–55°C to +125°C	E-44A

NOTES
[1]D = Ceramic DIP, E = Leadless Ceramic Chip Carrier.
[2]MIL-STD-883 version will be available; contact factory.

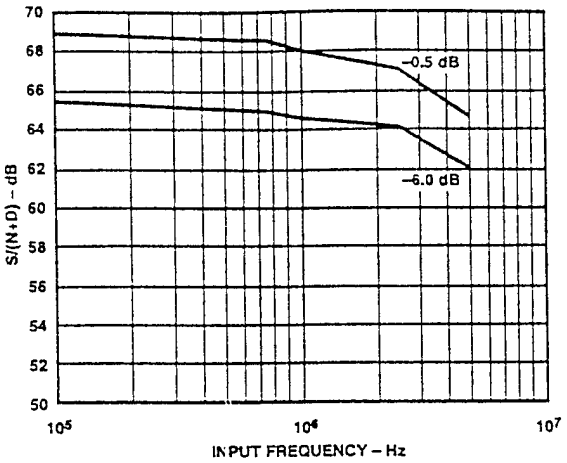


Figure 2. AD872A S/(N+D) Input Frequency

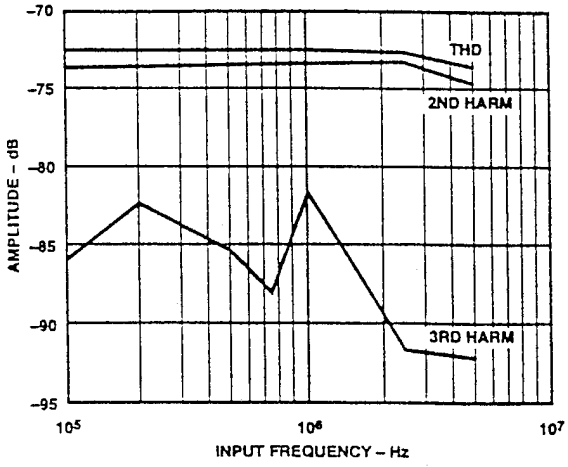


Figure 3. AD872A Distortion vs. Input Frequency, Full-Scale Input

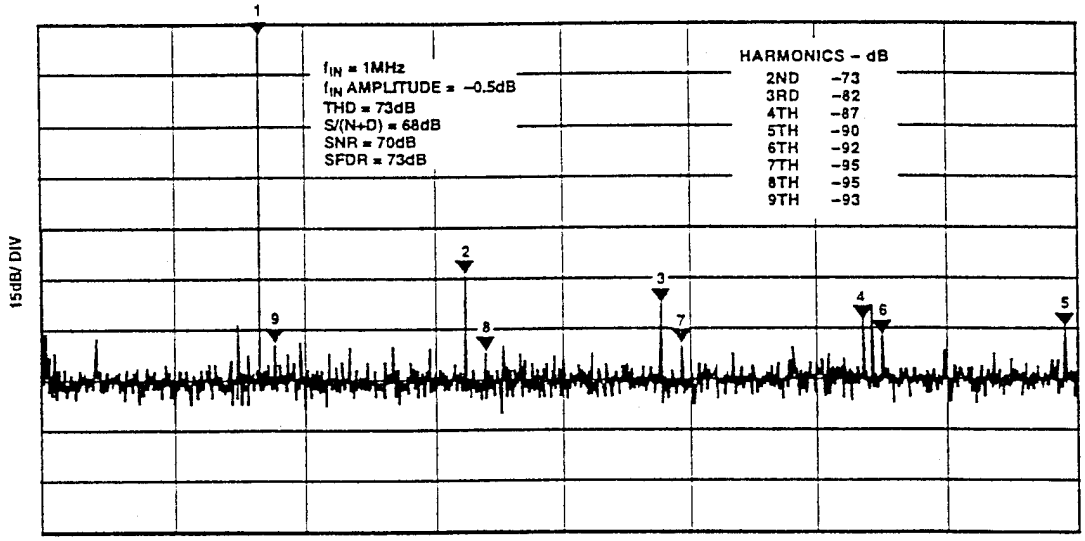


Figure 4. AD872A Typical FFT, f_{IN} = 1 MHz, f_{IN} Amplitude = –0.5 dB

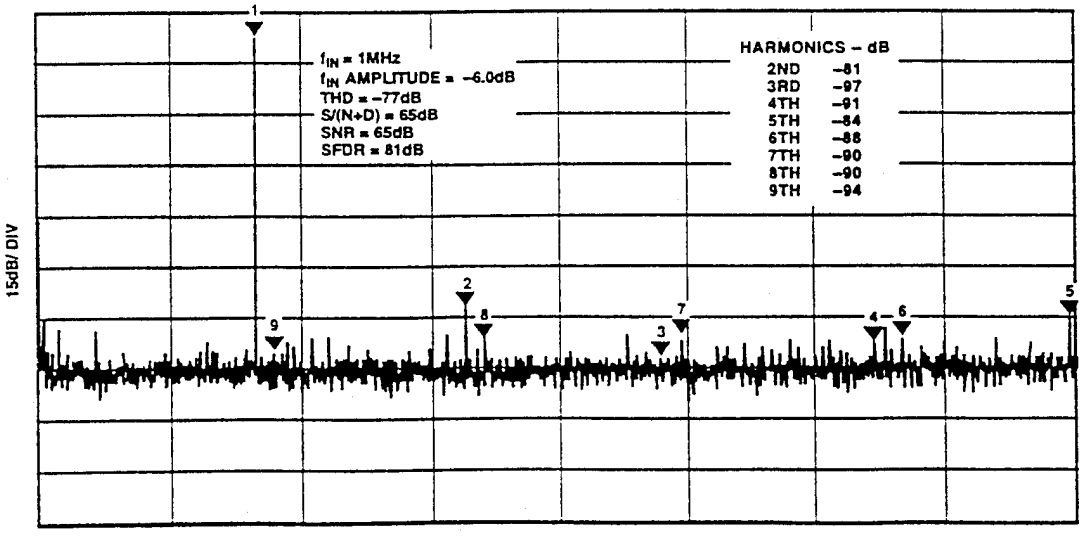


Figure 5. AD872A Typical FFT, f_{IN} = 1 MHz, f_{IN} Amplitude = –6 dB

AD872A–Dynamic Characteristics–Sample Rate: 10 MSPS

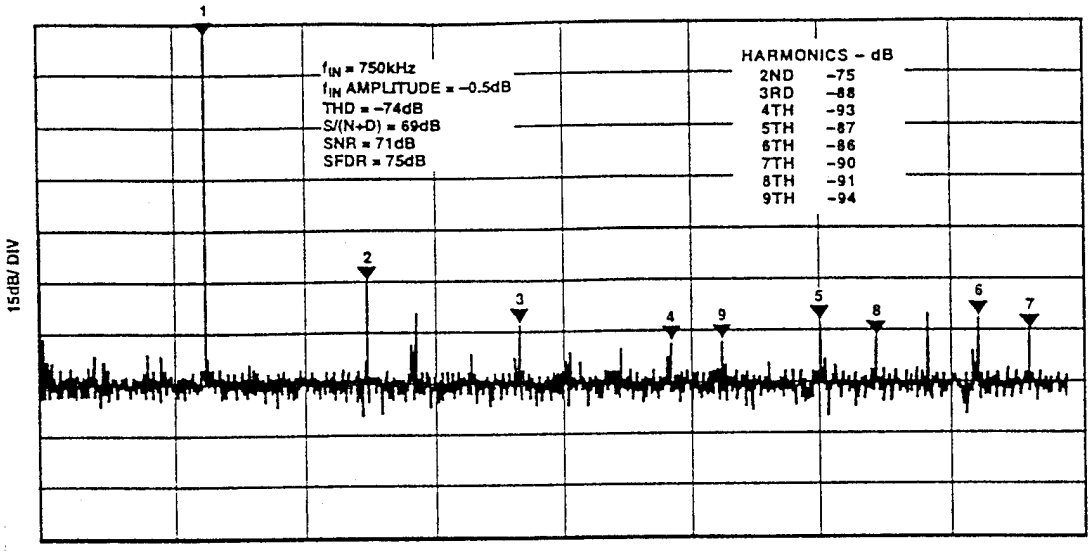


Figure 6. AD872A Typical FFT, f_{IN} = 750 kHz

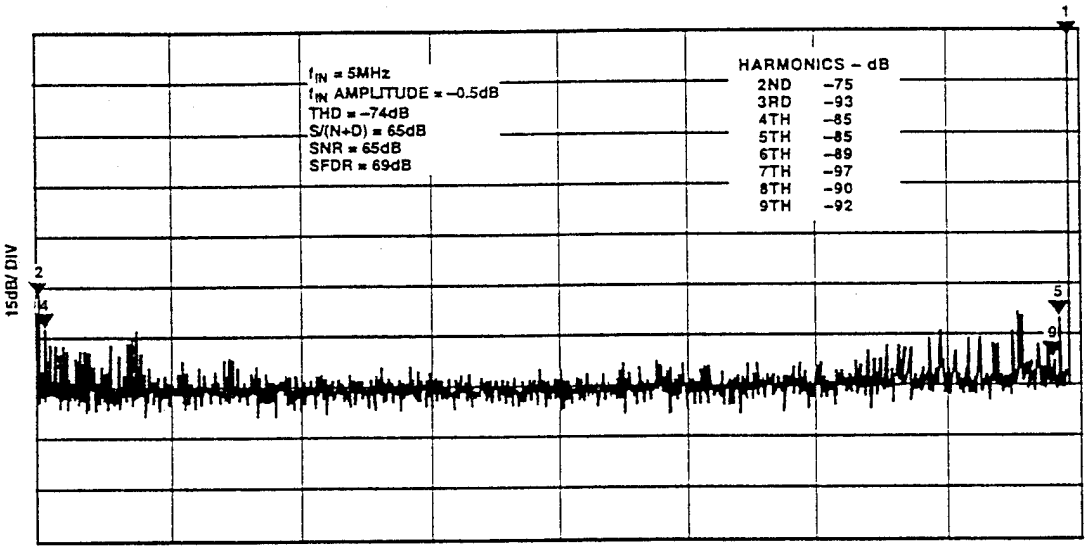


Figure 7. AD872A Typical FFT, f_{IN} = 5 MHz

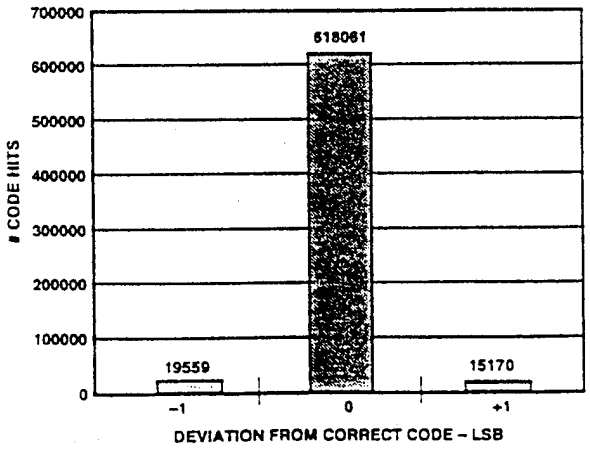


Figure 8. AD872A Output Code Histogram for DC Input

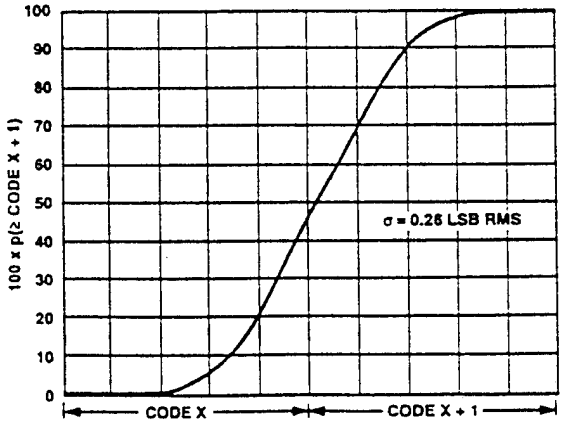


Figure 9. AD872A Code Probability at a Transition

THEORY OF OPERATION

The AD872A is implemented using a 4-stage pipelined multiple flash architecture. A differential input track-and-hold amplifier (THA) acquires the input and converts the input voltage into a differential current. A 4-bit approximation of the input is made by the first flash converter, and an accurate analog representation of this 4-bit guess is generated by a digital-to-analog converter. This approximation is subtracted from the THA output to produce a remainder, or residue. This residue is then sampled and held by the second THA, and a 4-bit approximation is generated and subtracted by the second stage. Once the second THA goes into hold, the first stage goes back into track to acquire a new input signal. The third stage provides a 3-bit approximation/subtraction operation, and produces the final residue, which is passed to a final 4-bit flash converter. The 15 output bits from the 4 flash converters are accumulated in the correction logic block, which adds the bits together using the appropriate correction algorithm, to produce the 12-bit output word. The digital output, together with overrange indicator, is latched into an output buffer to drive the output pins.

The additional THA inserted in each stage of the AD872A architecture allows pipelining of the conversion. In essence, the converter is converting multiple inputs simultaneously, processing them through the converter chain serially. This means that while the converter is capable of capturing a new input sample every clock cycle, it actually takes three clock cycles for the conversion to be fully processed and appear at the output. This "pipeline delay" is often referred to as latency, and is not a concern in most applications, however there are some cases where it may be a consideration. For example, some applications call for the A/D converter to be placed in a high speed feedback loop, where its input is servoed to provide a desired result at the digital output (e.g., offset calibration or zero restoration in video applications). In these cases the three clock cycle delay through the pipeline must be accounted for in the loop stability calculations. Also, because the converter is working on three conversions simultaneously, major disruptions to the part (such as a large glitch on the supplies or reference) may corrupt three data samples. Finally, there will be a minimum clock rate below which the THA droop corrupts the signal in the pipeline. In the case of the AD872A, this minimum clock rate is 10 kHz.

The high impedance differential inputs of the AD872A allow a variety of input configurations (see APPLYING THE AD872A), The AD872A converts the voltage difference between the V_{INA} and V_{INB} pins. For single-ended applications, one input pin (V_{INA} or V_{INB}) may be grounded, but even in this case the differential input can provide a performance boost: for example, for an input coming from a coaxial cable, V_{INB} can be tied to the shield ground, allowing the AD872A to reject shield noise as common mode. The high input impedance of the device minimizes external driving requirements and allows the user to externally select the appropriate termination impedance for the application.

The AD872A clock circuitry uses both edges of the clock in its internal timing circuitry (see spec page for exact timing requirements). The AD872A samples the analog input on the rising edge of the clock input. During the clock low time (between the falling edge and rising edge of the clock) the input THA is in track mode; during the clock high time it is in hold. System disturbances just prior to the rising edge of the clock may cause the part to acquire the wrong value, and should be minimized.

While the part uses both clock edges for its timing, jitter is only a significant issue for the rising edge of the clock (see CLOCK INPUT section).

APPLYING THE AD872A ANALOG INPUTS

The AD872A features a high impedance differential input that can readily operate on either single-ended or differential input signals. Table I summarizes the nominal input voltage span for both single-ended and differential modes, assuming a 2.5 V reference input.

Table I. Input Voltage Span

	V_{INA}	V_{INB}	V_{INA}–V_{INB}
Single-Ended	+1 V	GND	+1 V (Positive Full Scale)
	–1 V	GND	–1 V (Negative Full Scale)
Differential	+0.5 V	–0.5 V	+1 V (Positive Full Scale)
	–0.5 V	+0.5 V	–1 V (Negative Full Scale)

Figure 10 shows an approximate model for the analog input circuit. As this model indicates, when the input exceeds 1.6 V (with respect to AGND), the input device may saturate, causing the input impedance to drop substantially and significantly reducing the performance of the part. Input compliance in the negative direction is somewhat larger, showing virtually no degradation in performance for inputs as low as –1.9 V.

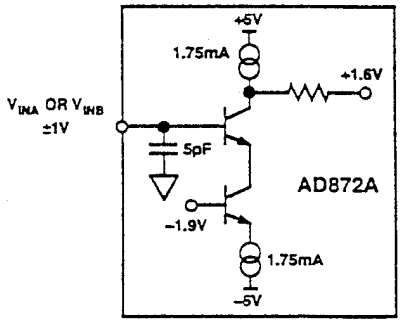


Figure 10. AD872A Equivalent Analog Input Circuit

Figure 11 illustrates the effect of varying the common-mode voltage of a –0.5 dB input signal on total harmonic distortion.

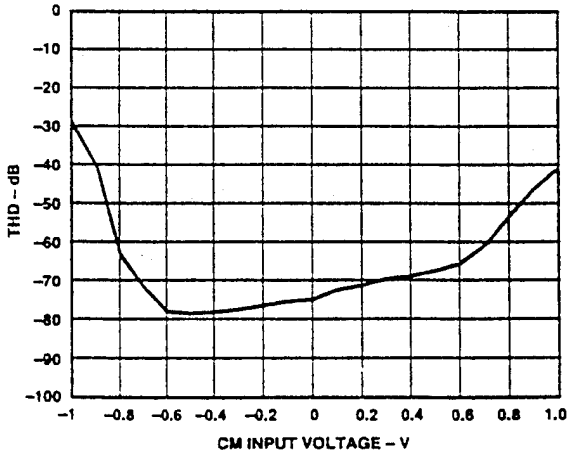


Figure 11. AD872A Total Harmonic Distortion vs. CM Input Voltage, f_{IN} = 1 MHz, FS = 10 MSPS

Figure 12 shows the common-mode rejection performance vs. frequency for a 1 V p-p common-mode input. This excellent common-mode rejection over a wide bandwidth affords the user the opportunity to eliminate many potential sources of input noise as common mode by using the differential input structure of the AD872A.

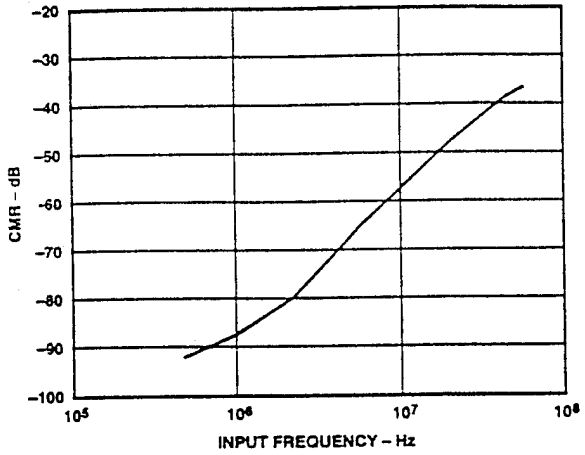


Figure 12. Common-Mode Rejection vs. Input Frequency, 1 V p-p Input

Figures 13 and 14 illustrate typical input connections for single-ended inputs.

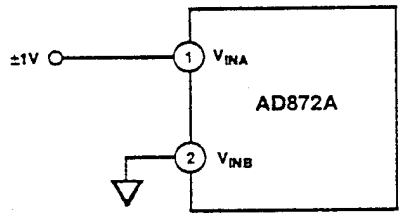


Figure 13. AD872A Single-Ended Input Connection

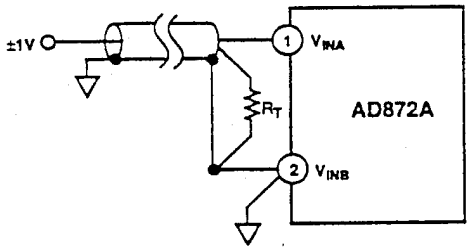


Figure 14. AD872A Single-Ended Input Connection Using a Shielded Cable

The cable shield is used as a ground connection for the V_{INB} input, providing the best possible rejection of the cable noise from the input signal. Note also that the high input impedance of the AD872A allows the user to select the termination impedance, be it 50 ohms, or some other value. Furthermore, unlike many flash converters, most AD872A applications will not require an external buffer amplifier. If such an amplifier is required, we suggest either the AD811 or AD9617.

Figure 15 illustrates how external amplifiers may be used to convert a single-ended input into a differential signal. The resistor values of 536 Ω and 562 Ω were selected to provide optimum phase matching between U1 and U2.

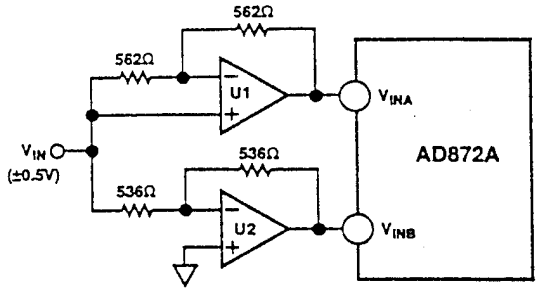


Figure 15. Single-Ended to Differential Connections; U1, U2 = AD811 or AD9617

The use of the differential input signal can help to minimize even-order distortion from the input THA where performance beyond –70 dB is desired.

Figure 16 shows the AD872A large signal (–0.5 dB) and small signal (–20 dB) frequency response.

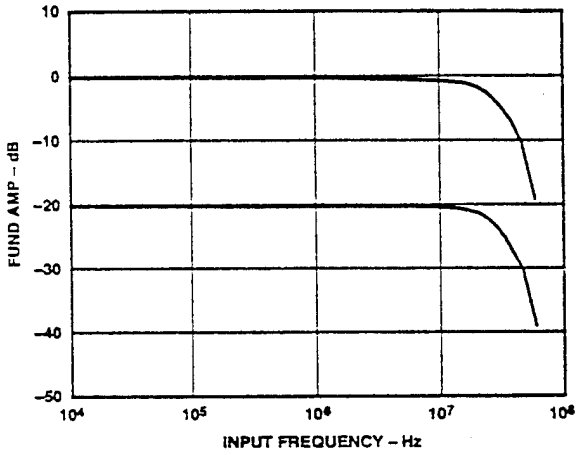


Figure 16. Full Power (–0.5 dB) and Small Signal Response (–20 dB) vs. Input Frequency

The AD872A's wide input bandwidth facilitates rapid acquisition of transient input signals: the input THA can typically settle to 12-bit accuracy from a full-scale input step in less than 40 ns. Figure 17 illustrates the typical acquisition of a full-scale input step.

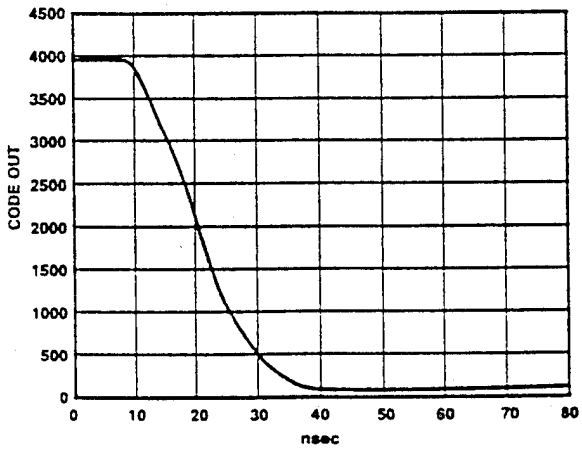


Figure 17. Typical AD872A Settling Time

The wide input bandwidth and superior dynamic performance of the input THA make the AD872A suitable for undersampling applications where the input frequency exceeds half the sample frequency. The input THA is designed to recover rapidly from input overdrive conditions, returning from a 50% overdrive in less than 40 ns.

Because of the THA's exceptionally wide input bandwidth, some users may find the AD872A is sensitive to noise at frequencies from 10 MHz to 50 MHz that other converters are incapable of responding to. This sensitivity can be mitigated by careful use of the differential inputs (see previous paragraphs). Additionally, Figure 18 shows how a small capacitor (10 pF-20 pF for 50 Ω terminated inputs) may be placed between V_{INA} and V_{INB} to help reduce high frequency noise in applications where limiting the input bandwidth is acceptable.

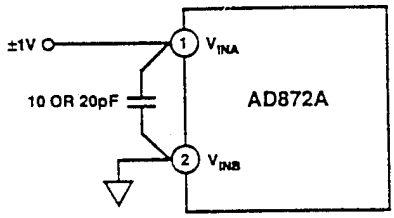


Figure 18. Optional High Frequency Noise Reduction

The AD872A will contribute its own wideband thermal noise. As a result of the integrated wideband noise (0.26 LSB rms, referred-to-input), applying a dc analog input may produce more than one code at the output. A histogram of the ADC output codes, for a dc input voltage, will be between one and three codes wide, depending on how well the input is centered on a given code and how many samples are taken. Figure 8 shows a typical AD872A code histogram, and Figure 9 illustrates the AD872A's transition noise.

REFERENCE INPUT

The nominal reference input should be 2.5 V, taken with respect to REFERENCE GROUND (REF GND). Figure 19 illustrates the equivalent model for the reference input: there is no clock or signal-dependent activity associated with the reference input circuitry, therefore, no "kickback" into the reference.

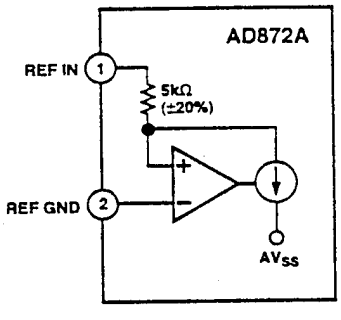


Figure 19. Equivalent Reference Input Circuit

However, in order to realize the lowest noise performance of the AD872A, care should be taken to minimize noise at the reference input.

The AD872A's reference input impedance is equal to 5 kΩ (±20%), and its effective noise bandwidth is 10 MHz, with a referred-to-input noise gain of 0.8. For example, the internal reference, with an rms noise of 28 μV (using an external 1 μF capacitor), contributes 24 μV (0.05 LSB) of noise to the transfer function of the AD872A.

The full-scale peak-to-peak input voltage is a function of the reference voltage, according to the equation:

$$(V_{INA} = V_{INB})\ Full\ Scale = 0.8 \times (V_{REF} - REF\ GND)$$

Note that the AD872A's performance was optimized for a 2.5 V reference input: performance may degrade somewhat for other reference voltages. Figure 20 illustrates the S/(N+D) performance vs. reference voltage for a 1 MHz, –0.5 dB input signal. Note also that if the reference is changed during a conversion, all three conversions in the pipeline will be invalidated.

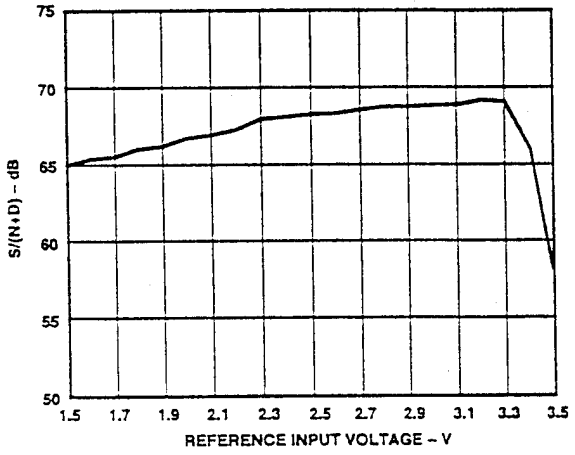


Figure 20. S/(N+D) vs. Reference Input Voltage, f_{IN} = 1 MHz, FS = 10 MHz

Table II summarizes various 2.5 V references suitable for use with the AD872A, including the onboard bandgap reference (see REFERENCE OUTPUT section).

Table II. Suitable 2.5 V References

	Drift (ppm/°C)	Initial Accuracy %
REF43B	6 (max)	0.2
AD680JN	10 (max)	0.4
Internal	30 (typ)	0.4

If an external reference is connected to REF IN, REF OUT must be connected to +5 V. This should lower the current in REF GND to less than 350 μA and eliminate the need for a 1 μF capacitor, although decoupling the reference for noise reduction purposes is recommended.

Alternatively, Figure 21 shows how the AD872A may be driven from other references by use of an external resistor. The external resistor forms a resistor divider with the on-chip 5 kΩ resistor to realize 2.5 V at the reference input pin (REF IN). A trim potentiometer is needed to accommodate the tolerance of the AD872A's 5 kΩ resistor.

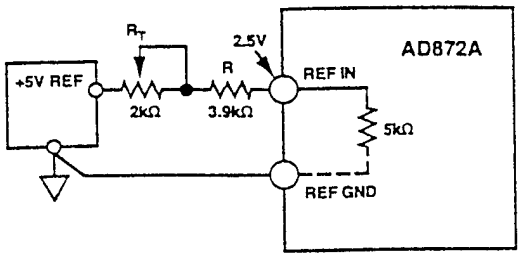


Figure 21. Optional +5 V Reference Input Circuit

REFERENCE GROUND

The REF GND pin provides the reference point for both the reference input, and the reference output. When the internal reference is operating, it will draw approximately 500 µA of current through the reference ground, so a low impedance path to the external common is desirable. The AD872A can tolerate a fairly large difference between REF GND and AGND, up to +1 V, without any performance degradation.

REFERENCE OUTPUT

The AD872A features an onboard, curvature compensated bandgap reference that has been laser trimmed for both absolute value and temperature drift. The output stage of the reference was designed to allow the use of an external capacitor to limit the wideband noise. As Figure 22 illustrates, *a 1 µF capacitor on the reference output is required for stability of the reference output buffer.* Note: If used, an external reference may become unstable with this capacitor in place.

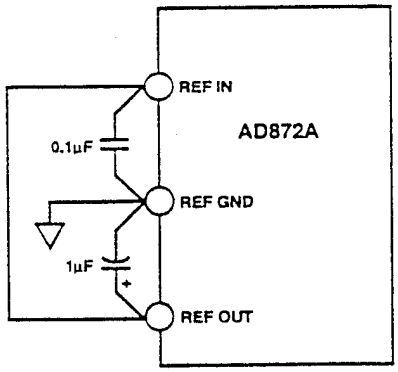


Figure 22. Typical Reference Decoupling Connection

With this capacitor in place, the noise on the reference output is approximately 28 µV rms at room temperature. Figure 23 shows the typical temperature drift performance of the reference, while Figure 24 illustrates the variation in reference voltage with load currents.

The output stage is designed to provide at least 2 mA of output current, allowing a single reference to drive up to four AD872A's, or other external loads. The power supply rejection of the reference is better than –54 dB at dc.

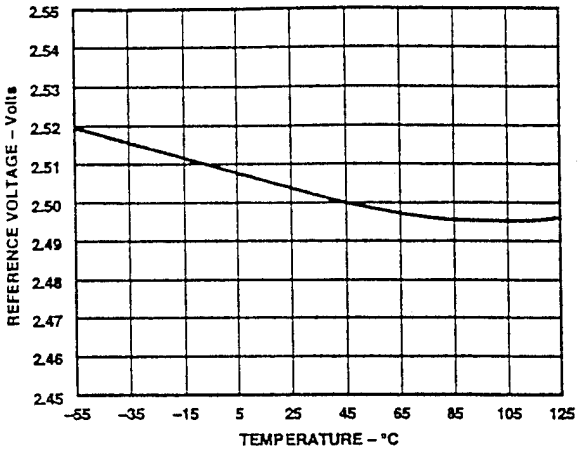


Figure 23. Reference Output Voltage vs. Temperature

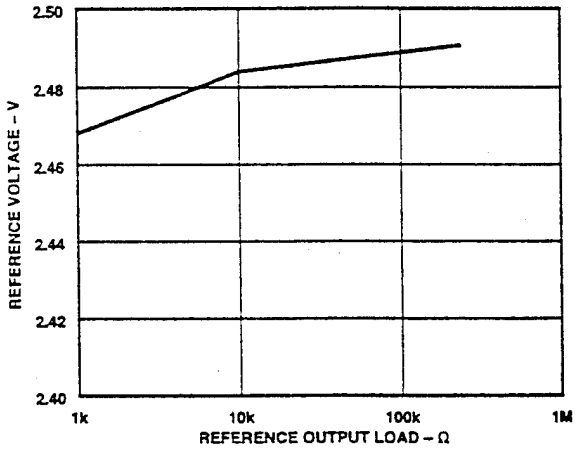


Figure 24. Reference Output Voltage vs. Output Load

DIGITAL OUTPUTS

In 28-pin packages, the AD872A output data is presented in twos complement format. Table III indicates offset binary and twos complement output for various analog inputs.

Table III. Output Data Format

Analog Input	Digital Output		
V_{INA}–V_{INB}	Offset Binary	Twos Complement	OTR
≥0.999756 V	1111 1111 1111	0111 1111 1111	1
0.999268 V	1111 1111 1111	0111 1111 1111	0
0 V	1000 0000 0000	0000 0000 0000	0
–1 V	0000 0000 0000	1000 0000 0000	0
–1.000244 V	0000 0000 0000	1000 0000 0000	1

Users requiring offset binary encoding may simply invert the $\overline{MSB}$ pin. In the 44-pin surface mount packages, both MSB and $\overline{MSB}$ bits are provided.

The AD872A features a digital out-of-range (OTR) bit that goes high when the input exceeds positive full scale or falls below negative full scale. As Table III indicates, the output bits will be set appropriately according to whether it is an out-of-range high

condition or an out-of-range low condition. Note that if the input is driven beyond +1.5 V, the digital outputs may not stay at +FS, but may actually fold back to midscale.

The AD872A's CMOS digital output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect S/(N+D) performance. Applications requiring the AD872A to drive large capacitive loads or large fanout may require additional decoupling capacitors on DRV_{DD} and DV_{DD}. In extreme cases, external buffers or latches could be used.

THREE-STATE OUTPUTS

The 44-pin surface mount AD872A offers three-state outputs. The digital outputs can be placed into a three-state mode by pulling the OUTPUT ENABLE (OEN) pin LOW. Note that this function is not intended to be used to pull the AD872A on and off a bus at 10 MHz. Rather, it is intended to allow the ADC to be pulled off the bus for evaluation or test modes. Also, to avoid corruption of the sampled analog signal during conversion (3 clock cycles), it is highly recommended that the AD872A be placed on the bus prior to the first sampling.

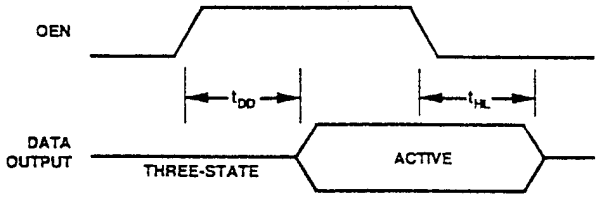


Figure 25. Three-State Output Timing Diagram

For timing budgetary purposes, the typical access and float delay times for the AD872A are 50 ns.

CLOCK INPUT

The AD872A internal timing control uses the two edges of the clock input to generate a variety of internal timing signals. The optimal clock input should have a 50% duty cycle; however, sensitivity to duty cycle is significantly reduced for clock rates of less than 10 megasamples per second.

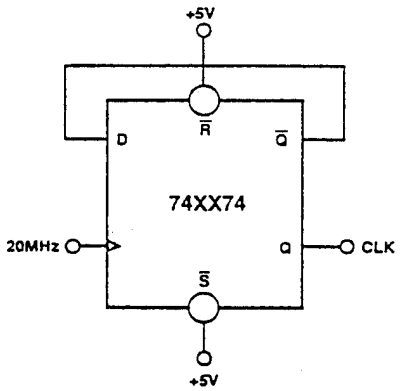


Figure 26. Divide-by-Two Clock Circuit

Due to the nature of on-chip compensation circuitry, the duty cycle should be maintained between 40% and 60% even for clock rates less than 10 Msps. One way to realize a 50% duty cycle clock is to divide down a clock of higher frequency, as shown in Figure 26.

In this case, a 20 MHz clock is divided by 2 to produce the 10 MHz clock input for the AD872A. In this configuration, the duty cycle of the 20 MHz clock is irrelevant.

The input circuitry for the CLKIN pin is designed to accommodate both TTL and CMOS inputs. The quality of the logic input, particularly the rising edge, is critical in realizing the best possible jitter performance for the part: the faster the rising edge, the better the jitter performance.

As a result, careful selection of the logic family for the clock driver, as well as the fanout and capacitive load on the clock line, is important. Jitter-induced errors become more pronounced at higher frequency, large amplitude inputs, where the input slew rate is greatest.

The AD872A is designed to support a sampling rate of 10 Msps; running at slightly faster clock rates may be possible, although at reduced performance levels. Conversely, some slight performance improvements might be realized by clocking the AD872A at slower clock rates. Figure 27 presents the S/(N+D) vs. clock frequency for a 1 MHz analog input.

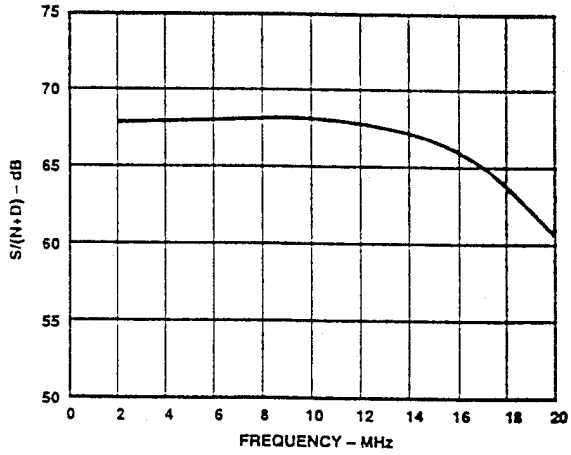


Figure 27. Typical S/(N+D) vs. Clock Frequency, f_{IN} = 1 MHz, Full-Scale Input

The power dissipated by the correction logic and output buffers is largely proportional to the clock frequency; running at reduced clock rates provides a slight reduction in power consumption. Figure 28 illustrates this tradeoff.

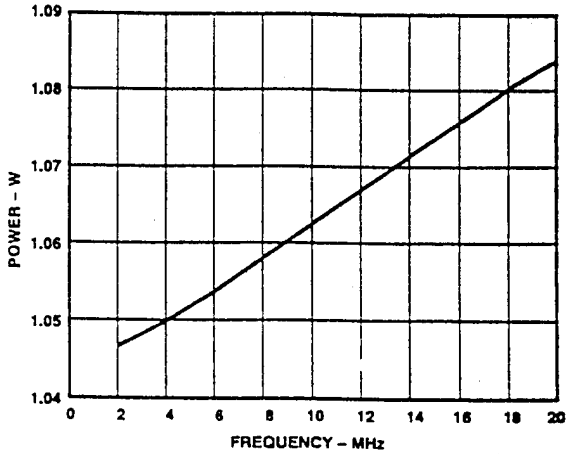


Figure 28. Typical Power Dissipation vs. Clock Frequency

ANALOG SUPPLIES AND GROUNDS

The AD872A features separate analog and digital supply and ground pins, helping to minimize digital corruption of sensitive analog signals. In general, AV_{SS} and AV_{DD}, the analog supplies, should be decoupled to AGND, the analog common, as close to the chip as physically possible. Care has been taken to minimize the signal dependence of the power supply currents; however, the analog supply currents will be proportional to the reference input. With REFIN at 2.5 V, the typical current into AV_{DD} is 85 mA, while the typical current out of AV_{SS} is 115 mA. Typically, 30 mA will flow into the AGND pin.

Careful design and the use of differential circuitry provide the AD872A with excellent rejection of power supply noise over a wide range of frequencies, as illustrated in Figure 29.

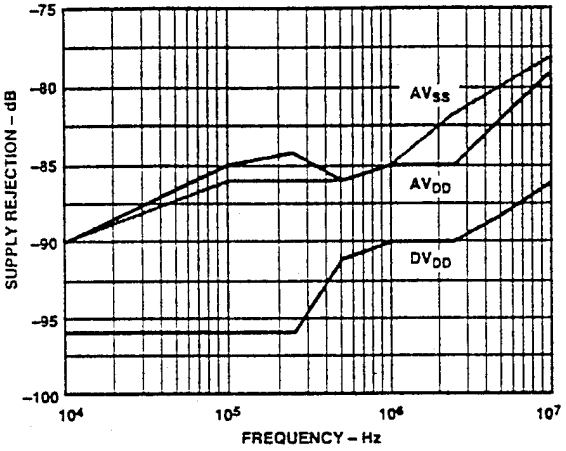


Figure 29. Power Supply Rejection vs. Frequency, 100 mV p-p Signal on Power Supplies

Figure 30 shows the degradation in SNR resulting from 100 mV of power supply ripple at various frequencies. As Figure 30 shows, careful decoupling is required to realize the specified dynamic performance. Figure 34 demonstrates the recommended decoupling strategy for the supply pins. Note that in extremely noisy environments, a more elaborate supply filtering scheme may be necessary.

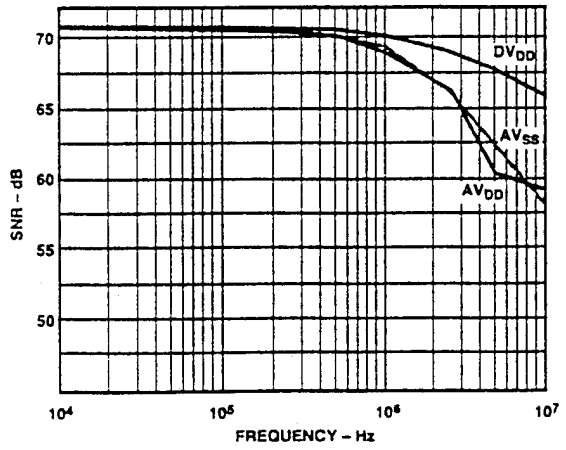


Figure 30. SNR vs. Supply Noise Frequency (f_{IN} = 1 MHz)

DIGITAL SUPPLIES AND GROUNDS

The digital activity on the AD872A chip falls into two general categories: CMOS correction logic, and CMOS output drivers. The internal correction logic draws relatively small surges of current, mainly during the clock transitions; in the 44-pin package, these currents flow through pins DGND and DV_{DD}. The output drivers draw large current impulses while the output bits are changing. The size and duration of these currents are a function of the load on the output bits: large capacitive loads are to be avoided. In the 44-pin package, the output drivers are supplied through dedicated pins DRGND and DRV_{DD}. Pin count constraints in the 28-pin packages require that the digital and driver supplies share package pins (although they have separate bond wires and on-chip routing). The decoupling shown in Figure 34 is appropriate for a reasonable capacitive load on the digital outputs (typically 20 pF on each pin). Applications involving greater digital loads should consider increasing the digital decoupling proportionately, and/or using external buffers/latches.

APPLICATIONS

OPTIONAL ZERO AND GAIN TRIM

The AD872A is factory trimmed to minimize zero error, gain error and linearity errors. In some applications the zero and gain errors of the AD872A need to be externally adjusted to zero. If required, both zero error and gain error can be trimmed with external potentiometers as shown in Figure 31. Note that gain error adjustments must be made with an external reference.

Zero trim should be adjusted first. Connect V_{INA} to ground and adjust the 10 kΩ potentiometer such that a nominal digital output code of 0000 0000 0000 (twos complement output) exists. Note that the zero trim should be decoupled and that the accuracy of the ±2.5 V reference signals will directly affect the offset.

Gain error may then be calibrated by adjusting the REF IN voltage. The REF IN voltage should be adjusted such that a +1 V input on V_{INA} results in the digital output code 01111 1111 1111 (twos complement output).

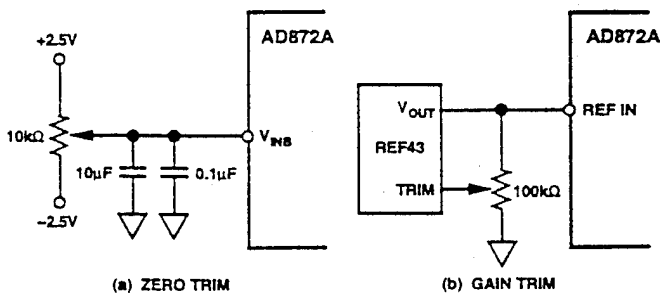


Figure 31. Zero and Gain Error Trims

DIGITAL OFFSET CORRECTION

The AD872A provides differential inputs that may be used to correct any offset voltages on the analog input. For applications where the input signal contains a dc offset, it may be advantageous to apply a nulling voltage to the V_{INB} input. Applying a voltage equal to the dc offset will maximize the full-scale input range and therefore the dynamic range. Offsets ranging from –0.7 V to +0.5 V can be corrected.

Figure 32 shows how a dc offset can be applied using the AD568 12-bit, high speed digital-to-analog converter (DAC). This circuit can be used for applications requiring offset adjustments on every clock cycle. The AD568 connection scheme is used to provide a –0.512 V to +0.512 V output range. The offset voltage must be stable on the rising edge of the AD872A clock input.

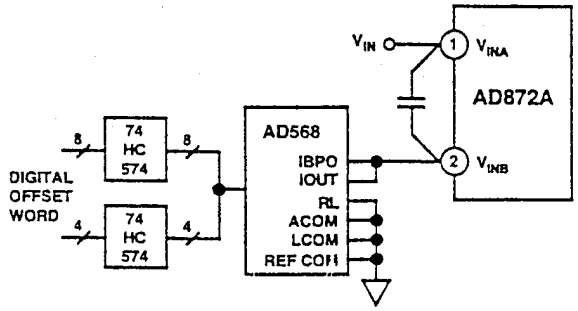


Figure 32. Offset Correction Using the AD568

UNDERSAMPLING USING THE AD872A AND AD9100

The AD872A's on-chip THA optimizes transient response while maintaining low noise performance. For super-Nyquist (undersampling) applications it may be necessary to use an external THA with fast track-mode slew rate and hold mode settling time. An excellent choice for this application is the AD9100, an ultrahigh speed track-and-hold amplifier.

In order to maximize the spurious free dynamic range of the circuit in Figure 33 it is advantageous to present a small signal to the input of the AD9100 and then amplify the output to the AD872A's full-scale input range. This can be accomplished with a low distortion, wide bandwidth amplifier such as the AD9617. The circuit uses a gain of 3.5 to optimize S/(N+D).

For small scale input signals (–20 dB, –40 dB), the AD872A performs better without the track-and-hold because slew-limiting effects are no longer dominant. To gain the advantages of the added track-and-hold, it is important to give the AD872A a full-scale input.

An alternative to the configuration presented above is to use the AD9101 track-and-hold amplifier. The AD9101 provides a built-in post amplifier with a gain of 4, providing excellent ac characteristics in conjunction with a high level of integration.

As illustrated in Figure 33, it is necessary to skew the AD872A sample clock and the AD9100 sample/hold control. Clock skew (t_S) is defined as the time starting at the AD9100's transition into hold mode and ending at the moment the AD872A samples. The AD872A samples on the rising edge of the sample clock, and the AD9100 samples on the falling edge of the sample/hold control. The choice of t_S is primarily determined by the settling time of the AD9100. The droop rate of the AD9100 must also be taken into consideration. Using these values, the ideal t_S is 17 ns. When choosing clock sources, it is extremely important that the front end track-and-hold sample/hold control is given a very low jitter clock source. This is not as crucial for the AD872A sample clock, because it is sampling a dc signal.

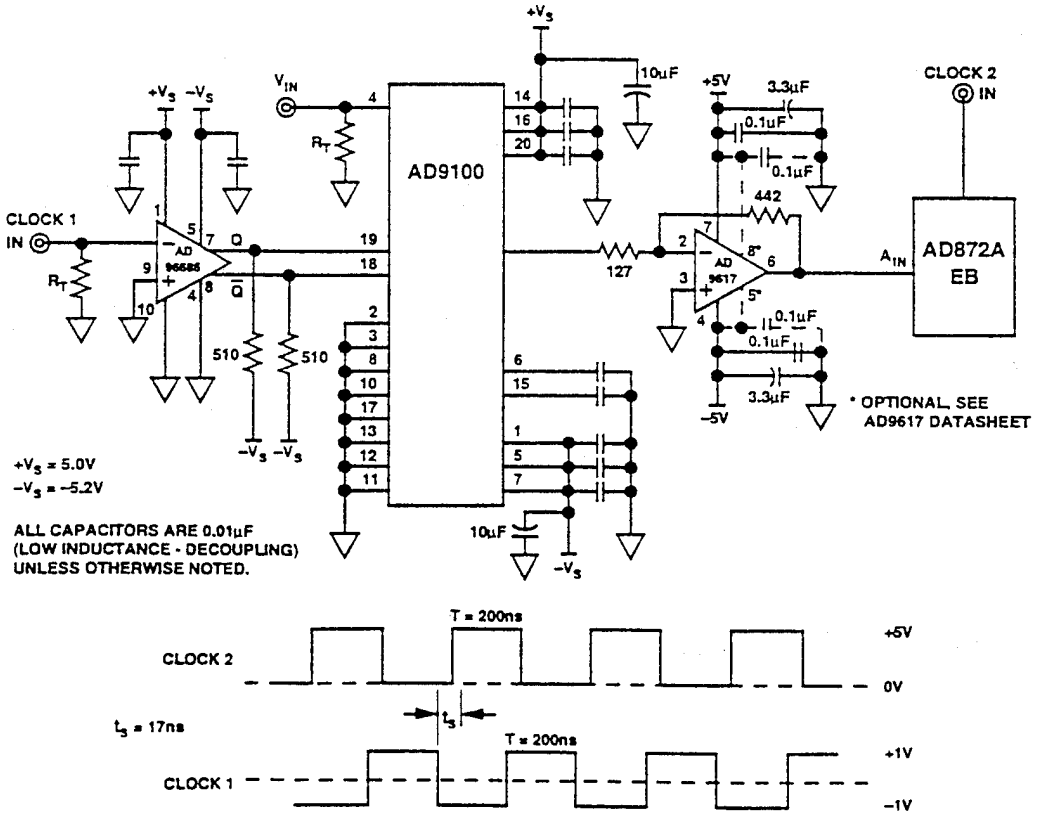


Figure 33. Undersampling Using the AD872A and AD9100

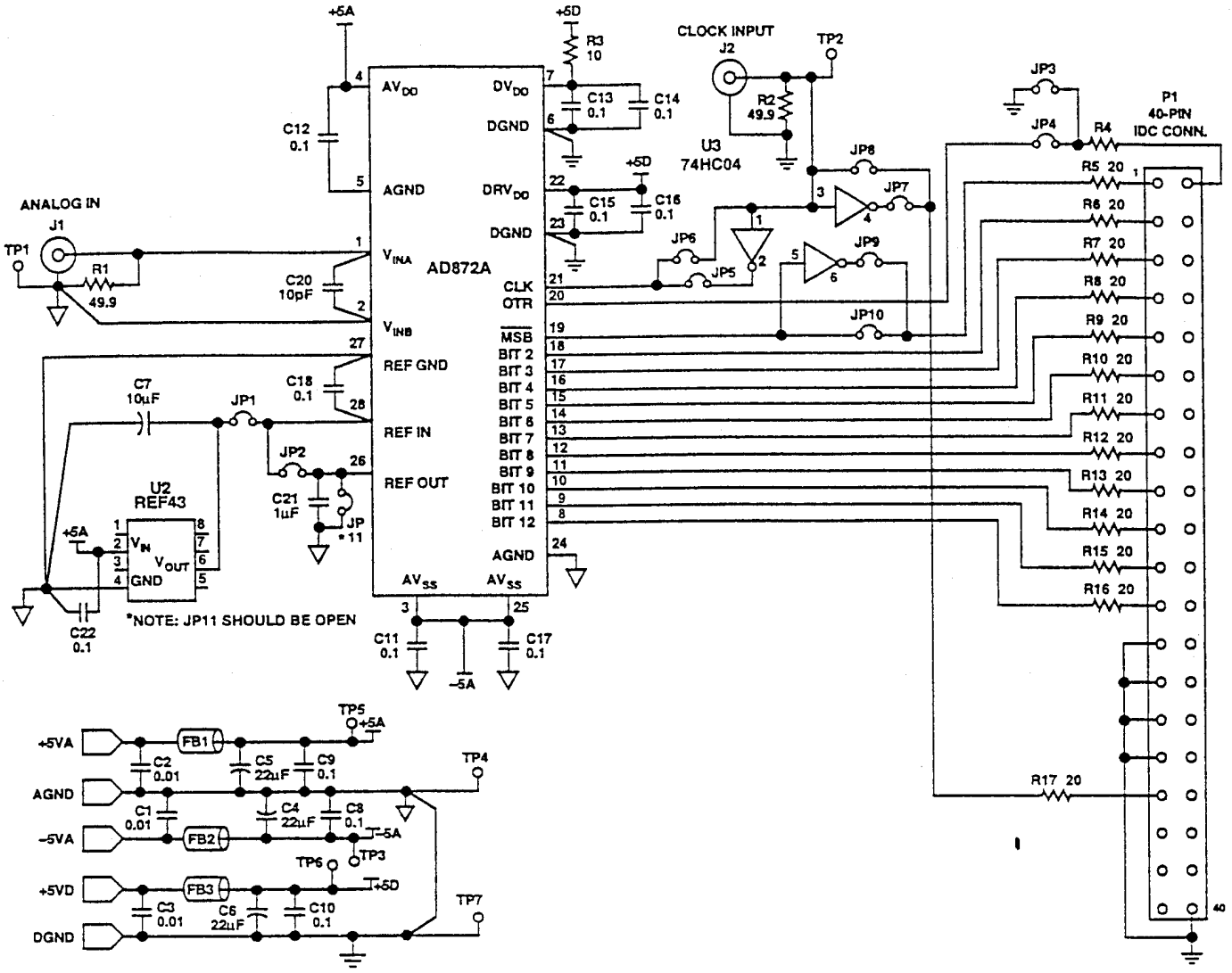


Figure 34. AD872A/AD871 Evaluation Board Schematic

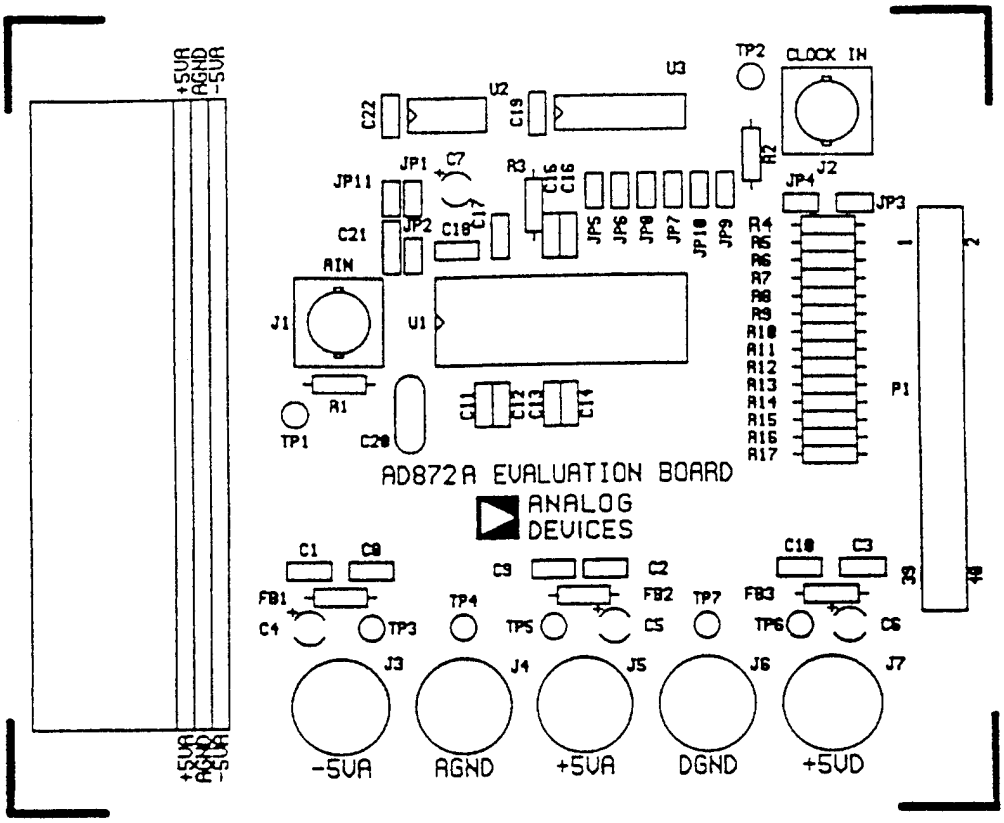


Figure 36. Silkscreen Layer PCB Layout (Not Shown to Scale)

Table IV. Components List

Reference Designator	Description	Quantity
R1, R2	Resistor, 1%, Metal Film, 49.9 Ω	2
R3	Resistor, 1%, Metal Film, 10	1
R4–R17	Resistor, 1%, Metal Film, 20	14
C1–C3	SMD Chip Capacitor, 0.01 µF	3
C4–C6	Capacitor, Tantalum, 22 µF	3
C7	Capacitor, Tantalum, 10 µF	1
C8–C19, C22	SMD Chip Capacitor, 0.1 µF	13
C20	Capacitor, Mica, 10 pF	1
C21	Capacitor, Ceramic, 1 µF	1
U1	AD872A	1
U2	REF43B	1
U3	74HC04N	1
FB1–FB3	Ferrite Bead	3
J1, J2	BNC Jack	2
JP2, 3, 5, 7, 10	Jumpers	5
JP1–JP11	Headers	11
P1	40-Pin IDC Connector	1

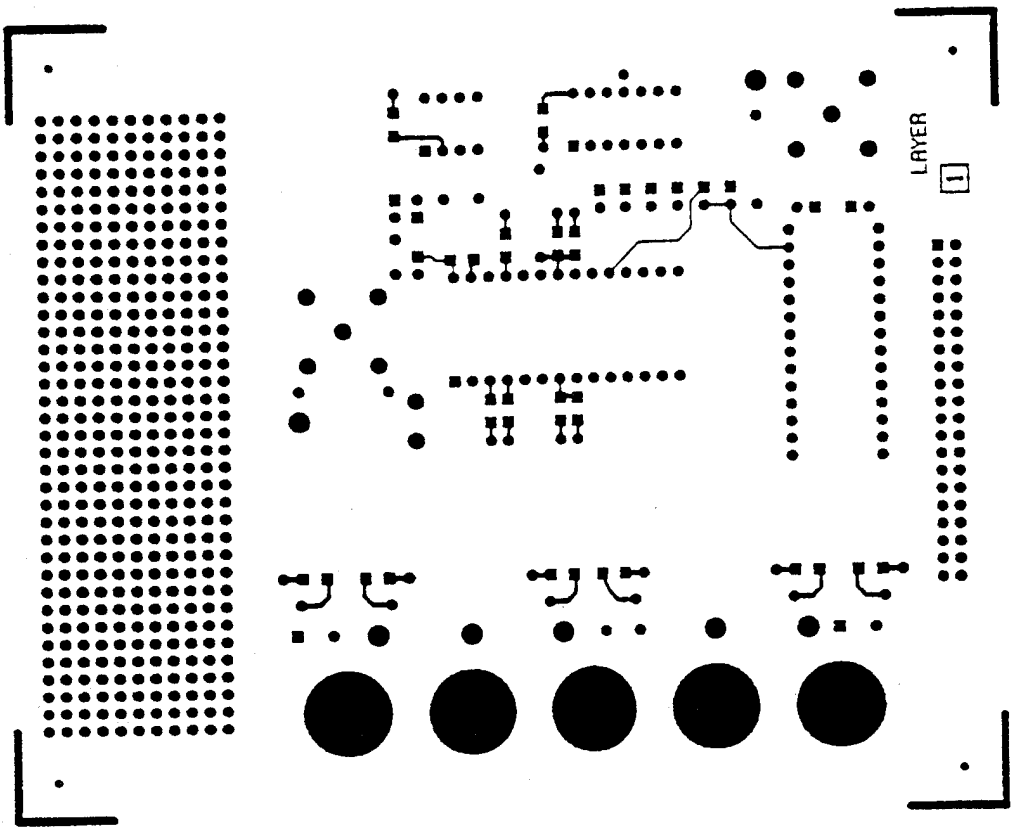


Figure 37. Component Side PCB Layout (Not Shown to Scale)

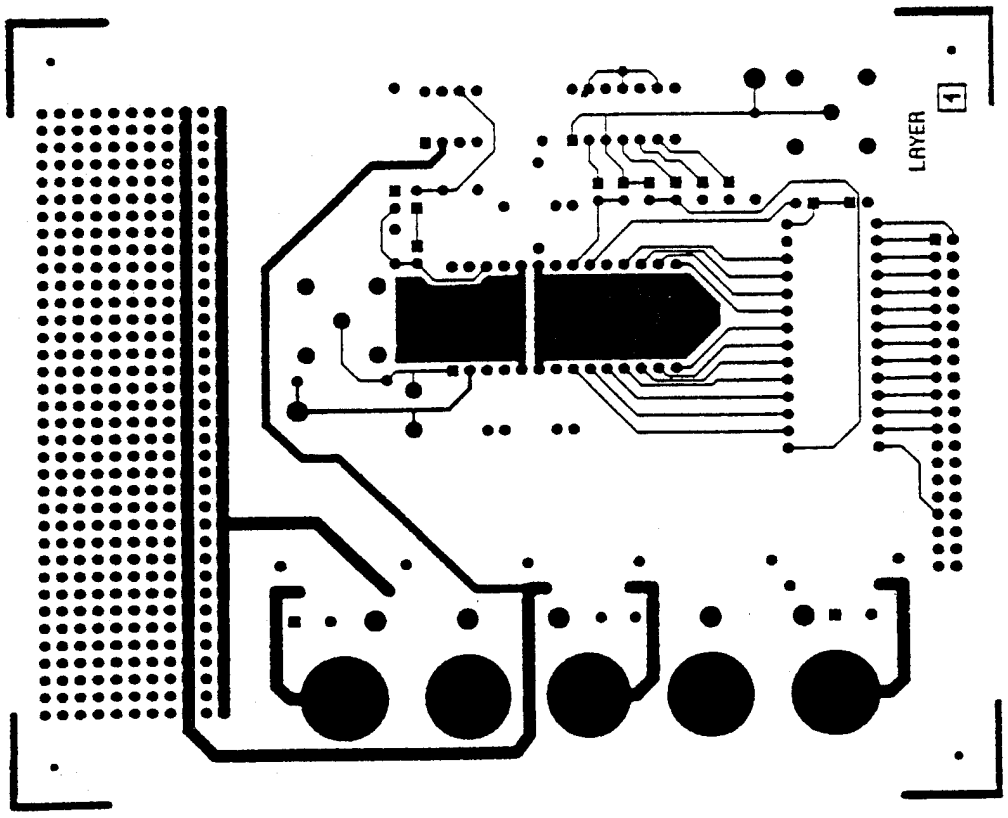


Figure 38. Solder Side PCB Layout (Not Shown to Scale)

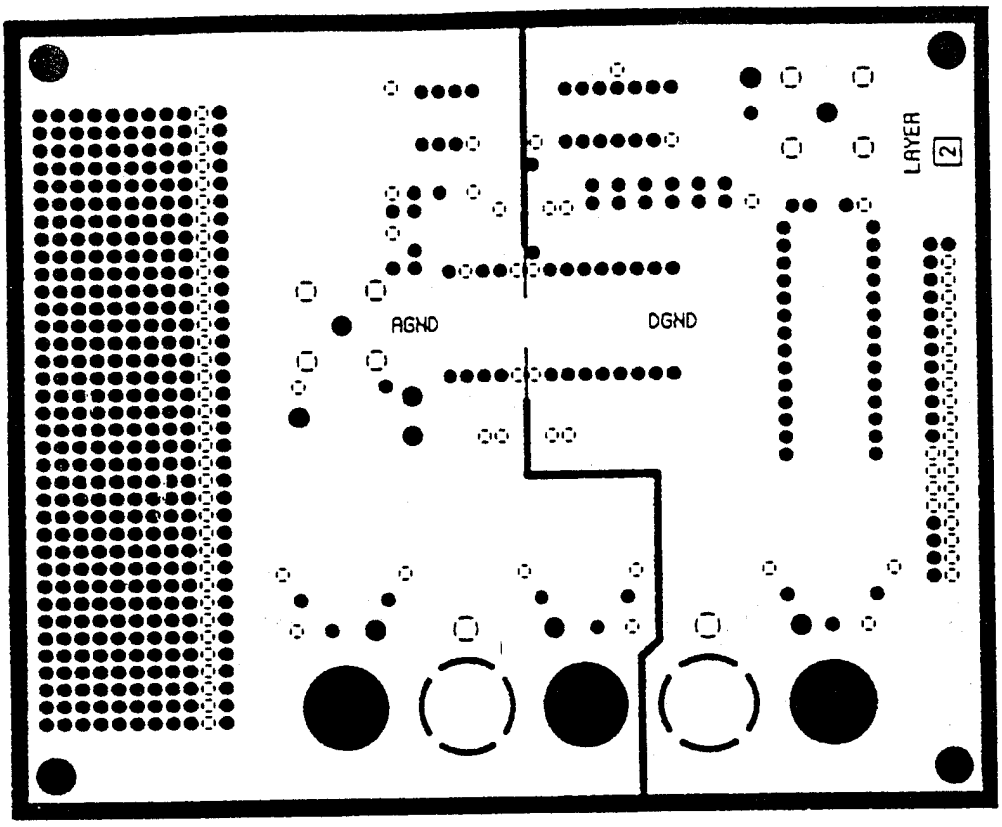


Figure 39. Ground Layer PCB Layout (Not Shown to Scale)

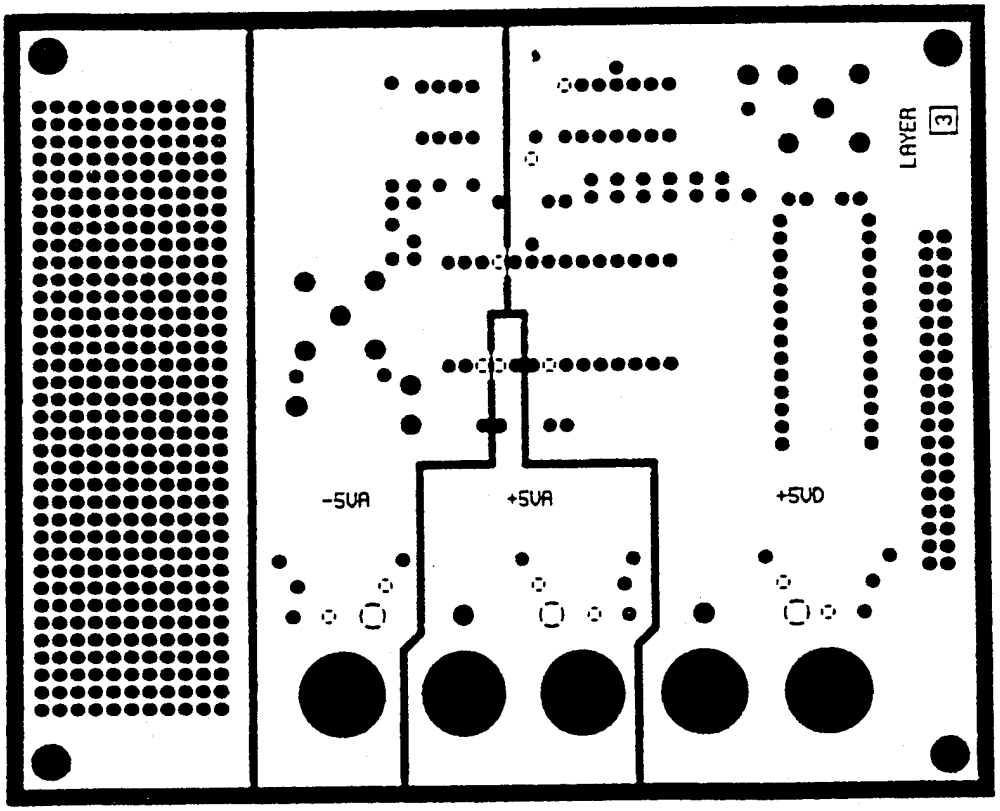
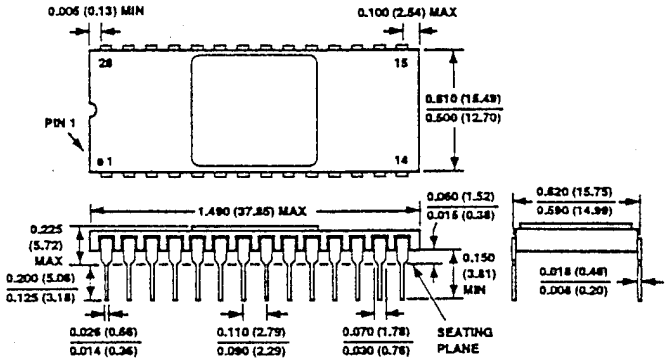


Figure 40. Power Layer PCB Layout (Not Shown to Scale)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Pin Sidebrazed DIP (D-28)



44-Terminal LCC (E-44A)